Hoogfrequente karakterisering van ingebedde componenten in gedrukte schakelingen

High-Frequency Characterization of Embedded Components in Printed Circuit Boards

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Voor Gijs

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Dankwoord

Een man met een grote witte haardos heeft ooit gezegd dat alles relatief is. Zo is het ook met dit doctoraat. En dan doel ik niet op de inhoudelijke kwaliteit of op de discussie over de waarde van een dergelijke titel, waarover ik wijselijk mijn mening hier niet ga neerschrijven. Het behalen van een doctoraat valt in het niets in verhouding tot het verlies van een vriend. We blijven je missen, Gijsje.

Als je gedurende bijna zeven (7!) jaar aan je doctoraat werkt, dan zijn er uiteraard heel wat mensen die in de loopt van de tijd hun steentje bijdragen. Veelal gebeurde dit bewust, maar af en toe kon een onbewuste actie ook een grote steun betekenen. Hierbij denk ik vooral aan mijn familie en *mien moaten*. Tot spijt van wie het benijdt, ga ik hier geen lange lijst van namen opnoemen. Niet zozeer omdat ik vrees van iemand te vergeten, maar eerder omdat ik weet dat de mensen die mij echt geholpen hebben, dit niet deden om op deze pagina vermeld te worden.

Een lijdensweg zou ik een doctoraat niet noemen, maar het verloopt toch met hoogtes en laagtes. Gelukkig kan er ten gepaste tijde beroep gedaan worden op een reeks superhelden om problemen van praktische en minder praktische aard op te lossen: Laser Man, Ms Proper, Etch Man, Super Peacock, Handy Man, Admin Woman, Comsol Guy, Assembly Man and Plating Girl. Ook zonder de steun van bovenaf, al dan niet met kostuumsvest, was dit doctoraat niet tot stand gekomen. Daarnaast wil ik ook nog *Ze Djermans* speciaal vermelden voor de hulp bij het verwezenlijken van de testkaart.

Volleyballers aller landen, en bij uitbereiding ook andere ploegsporters, hebben meermaals bewezen dat *together each achieves more*. De vele leuke momenten, recreatief en competitief, op en naast het veld, bacterieel of viraal, zorgden voor een welgekomen afwisseling.

Maarten Cauwe
22 juni 2010

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List of Acronyms

3D	three-dimensional.
3G	third generation.
AC	alternating current.
B2IT	buried bump interconnection technology.
BBUL	bumpless build-up layer.
BGA	ball grid array.
BT	bismaleimide triazine.
CAD	computer aided design.
CIP	chip in polymer.
CMOS	complementary metaloxidesemiconductor.
COB	chip on board.
CPU	central processing unit.
CSP	chip-scale package.
CTE	coefficient of thermal expansion.
CUP	circuit under pad.
DAP	die attach pad.
DAT	die attach tape.
DBG	dicing by grinding.
DC	direct current.
DCA	direct chip attach.
DDR	double data rate.
DIP	dual in-line package.
DRAM	dynamic random access memory.
DSP	digital signal processor.

EMI	electromagnetic interference.
ESL	equivalent series inductance.
ESR	equivalent series resistance.
eWLB	embedded wafer level ball grid array.
eWLP	embedded wafer level package.
FBGA	fine-pitch ball grid array.
FCBGA	flip-chip ball grid array.
fcCSP	flip-chip chip-scale package.
FDTD	finite-difference time-domain.
FEM	finite element method.
FPM	four-point measurement.
FRTV	radio frequency test vehicle.
GaAs	gallium arsenide.
GPS	global positioning system.
GSM	global system for mobile communications.
HDI	high-density integration.
HSDPA	high-speed downlink packet access.
I/O	input/output connection.
IBIS	input/output buffer information specification.
IC	integrated circuit.
IMB	integrated module board.
IPC	institute for printed circuits (deprecated).
ITRS	international technology roadmap for semiconductors.
JEDEC	joint electron device engineering council.
KGD	known-good die.
L/S	line width/spacing.
LAN	local area network.
LDI	laser direct imaging.
LGA	land grid array.

LQFP	low-profile quad flat package.
LRM	line reflect match.
MEMS	micro-electro-mechanical systems.
ML-TRL	multiline thru reflect line.
MLF	MicroLeadFrame (Amkor QFN).
MoL	method of lines.
MoM	method of moments.
MQFP	metric quad flat pack.
NOR	logical "not-or".
PA	power amplifier.
PBGA	plastic ball grid array.
PCB	printed circuit board.
PDN	power delivery network.
PGA	pin grid array.
PoP	package-on-package.
PRBG	pseudo-random bit generator.
PTH	plated through-hole.
QFN	quad flat no leads.
QFP	quad flat pack.
RCC	resin coated copper.
RCP	redistribution chip package.
RDL	redistribution layer.
RF	radio frequency.
RH	relative humidity.
SAC	tin silver copper (solder).
SDA	spectral domain approach.
SiB	system-in-board.
SiP	system-in-package.
SLR	single-layer reduction.
SMD	surface-mount device.
SMT	surface-mount technology.
SO	small outline.

SoC	system-on-chip.
SOIC	small outline integrated circuit.
SOLT	short open load thru.
SPICE	simulation program with integrated circuit emphasis.
SRAM	static random access memory.
TDR	time domain reflectometer.
TEM	transverse electromagnetic.
TM	transverse magnetic.
TRL	thru reflect line.
TSV	through-silicon via.
TTC	thermal test chip.
UBM	under bump metallization.
UMTS	universal mobile telecommunications system.
UV	ultraviolet.
VRM	voltage regulator module.
Wi-Fi	wireless network.
WL-CSP	wafer level chip-scale package.
WLP	wafer level packaging.

List of Symbols

A	area.
A_f	An-factor.
A_z	magnetic potential.
C	capacitance.
C_0	characteristic capacitance.
C_B	bulk capacitance of the power plane.
C_N	neutral capacitance.
C_d	on-die decoupling capacitance.
C_i	decoupling capacitance of branch i.
C_l	line capacitance.
C_p	on-package decoupling capacitance.
C_{MS}	microstrip capacitance.
C_{PP}	parallel-plate capacitance.
C_{TOT}	total capacitance.
C_{eff}	effective capacitance.
C_{ex}	excessive capacitance.
C_{tot}	total capacitance.
E_t	transverse component of the electric field.
E_z	longitudinal component of the electric field.
G	conductance.
G_{tot}	total conductance.
H_t	transverse component of the magnetic field.
H_z	longitudinal component of the magnetic field.
I	current.
I_c	current on the centre conductor.
J_s	surface current density.
K_b	backwards coupling factor.
L	inductance.

L_N	neutral inductance.
L_i	parasitic inductance of decoupling branch i.
L_l	line inductance.
L_{ext}	external inductance.
L_{ex}	excessive inductance.
L_{int}	internal inductance.
L_{p1}	parasitic inductance between die and package.
L_{p2}	parasitic inductance of the on-package decoupling capacitor.
L_{tot}	total inductance.
M_i	measured cascade parameters for line i.
Q	total charge.
R	resistance.
R_l	line resistance.
R_{AC}	AC resistance.
R_{Cu}	resistance per unit length of the copper layer.
R_{DC}	DC resistance.
R_{Si}	resistance per unit length of the silicon layer.
R_{tot}	total resistance.
S_{Cu}	area of the copper domain(s).
S_{Si}	area of the silicon domain(s).
S_{ij}	element i, j of the S-parameter matrix.
T_g	glass transition temperature.
T_i	cascade parameters of the line standard i.
V	voltage.
V_{OPEN}	vertical opening of the eye diagram.
X	left error box.
Y	admittance.
Y_0^i	characteristic admittance of layer i.
Y_{in}^i	input admittance of layer i.
Z	impedance.
Z_0	characteristic impedance.
Z_0^i	characteristic impedance of layer i.
Z_C	characteristic impedance.
Z_l	line impedance.
Z_s	surface impedance.
Z_{PDN}	impedance of the power delivery network.
Z_{ij}	element i, j of the impedance matrix.

$Z_{in,ll}$	input impedance of the lowest layer.
Z_{in}^{i}	input impedance of layer i.
Z_{pp}	parallel-plate impedance.
$\Delta\alpha$	relative error of the total loss.
$\Delta\epsilon_{eff}$	relative error of the effective dielectric constant.
$\Im(X)$	imaginary part of X.
Φ_{eff}	effective phase difference.
$\Re(X)$	real part of X.
α	loss, real part of propagation constant.
α_c	conductive loss.
α_d	dielectric loss.
$\bar{Y}$	right error box.
β	phase shift, imaginary part of propagation constant.
δ	depth of penetration.
δ_{Cu}	depth of penetration into copper.
δ_{Si}	depth of penetration into silicon.
ϵ	dielectric constant.
ϵ'	real part of the dielectric constant.
ϵ''	imaginary part of the dielectric constant.
$\epsilon^{\star}$	complex dielectric constant.
ϵ_0	permittivity of free-space.
ϵ_i	dielectric constant of the insulating layer.
ϵ_m	dielectric constant of the metal layer.
ϵ_r	relative dielectric constant.
ϵ_s	dielectric constant of the semiconducting layer.
ϵ_{DAT}	relative dielectric constant of the die attach tape.
ϵ_{RCC}	relative dielectric constant of the resin coated copper.
ϵ_{SM}	relative dielectric constant of the solder mask.
ϵ_{Si}	relative dielectric constant of the silicon.
ϵ_{eff}	effective dielectric constant.
$\epsilon_{r,eff}$	effective relative dielectric constant.
$\epsilon_{r,eq}$	equivalent relative dielectric constant.
$\epsilon_{r\infty}$	optical value of the Maxwell-Wagner permittivity.
ϵ_{rs}	static value of the Maxwell-Wagner permittivity.

η	wave impedance.
η_i	intrinsic impedance.
γ	propagation constant.
γ_i	propagation constant in material i.
γ_m	propagation constant in metal layer.
γ_{meas}	propagation constant extracted from the measurements.
γ_{model}	propagation constant extracted from the model.
$\hat{C}$	complex circuit capacitance.
$\hat{L}$	complex circuit inductance.
$\mathbf{E}$	electric field.
$\mathbf{H}$	magnetic field.
μ	permeability.
μ'	real part of the permeability.
μ''	imaginary part of the permeability.
$\mu^\star$	complex permeability.
μ_0	permeability of free-space.
μ_r	relative permeability.
μ_{eff}	effective permeability.
ω	angular frequency.
ϕ	electric potential.
σ	conductivity.
σ_{Cu}	copper conductivity.
σ_{Si}	silicon conductivity.
$\tan\delta$	loss tangent.
$\tan\delta_{eff}$	effective loss tangent.
$\tan\delta_{eq}$	equivalent loss tangent.
τ	time constant.
τ_e	time constant for the dielectric relaxation.
τ_s	time constant for the interfacial polarization relaxation.
f	frequency.
f_0	transition frequency for the slow-wave mode region.
f_e	dielectric relaxation frequency.
f_s	interfacial polarization relaxation frequency.
f_{01}	horizontal board resonant frequency.
f_{10}	vertical board resonant frequency.

f_δ	transition frequency for the skin effect region.
f_{res}	resonant frequency.
h	height.
h_s	height of the semiconducting layer.
h_{DAT}	height of the die attach tape layer.
h_{RCC}	height of the resin coated copper layer.
h_{RMS}	root-mean-square roughness height.
h_{Si}	height of the silicon layer.
h_{eff}	effective height.
i_0	modal current.
k_p	proximity factor for the conductive loss.
k_r	roughness factor for the conductive loss.
l_i	length of line standard i.
t	thickness.
t_r	rise time.
t_{OPEN}	horizontal opening of the eye diagram.
v_0	modal voltage.
w	width.
w_{eff}	effective width.
w_e	equivalent width.

Nederlandse samenvatting

Het inbedden van elektronische chips is een driedimensionale verpakkingstechnologie die als alternatief kan dienen voor draad- en flip-chip verbindingen. De processen voor het inbedden van chips kunnen ingedeeld worden in twee categorieën. Een eerst groep wordt samengebracht onder de noemer "uitwaaierende verpakkingstechnieken op waferniveau". De beschikbare oppervlakte bovenop de chip wordt uitgebreid door de chip in te bedden in een polymeer matrix. Daartegenover staat het rechtstreeks inbedden van actieve en passieve componenten in gedrukte schakelingen. Met deze, meer systeemgeoriënteerde benadering wordt het gebruik van een verpakking volledig vermeden. Een eerste methode voor het rechtstreeks inbedden plaatst de chips ondersteboven in de binnenlagen van de printkaart, gebruik makend van holtes of geponste openingen in de prepreg. Een alternatieve aanpak gaat uit van zeer dunne chips die ingebed worden in opbouwlagen van printkaarten met hoge dichtheid, waarbij de verbindingen naar de chips gerealiseerd worden met microvia technologie.

Het gebruik van ingebedde componenten resulteert in een driedimensionale verbindingsstructuur. Hierdoor wordt niet enkel de lengte van de verbinding tussen de chip en de printkaart verkleind, maar eveneens de lengte van het signaalpad tussen de verschillende componenten. Terminatieweerstanden of ontkoppelcapaciteiten worden rechtstreeks boven de bijhorende paden van de chip geplaatst, terwijl hogesnelheidscommunicatie tussen twee geïntegreerde schakelingen verwezenlijkt wordt door de tweede chip bovenop de ingebedde chip te plaatsen. De vrijgekomen ruimte op de printkaart kan gebruikt worden om eventuele onregelmatigheden in het signaalpad te verhelpen en zo de overdracht van de hoogfrequente signalen te verbeteren. Wanneer de totale beschikbare ruimte beperkt is, of wanneer het contactpad zich in het centrum van de chip bevindt, kunnen hogesnelheidsverbindingen over de chip heen lopen. De invloed van ingebedde chips op de impedantie en de verliezen van baantjes die over en onder de chips lopen wordt in detail bestudeerd, met als doel het gebruik van gecontroleerde impedantie in combinatie met ingebedde componenten mogelijk te maken. De fijnmazige verbindingen op de chip zelf kunnen, samen met een eventuele herdistributielaag, de invloed van de halfgeleidende laag afschermen en een soort virtueel grondvlak vormen. In deze thesis wordt

een breedband model voor dergelijke meerlaagse microstrip lijnen ontwikkeld en geverifieerd aan de hand van simulaties en metingen.

De verbinding naar de ingebedde chips en de overspraak tussen signalen op de ingebedde component en zijn omgeving maken eveneens deel uit van de hoogfrequente karakterisering van ingebedde componenten. Als gevolg van de zeer dunne laag diëlektricum boven de chip is het mogelijk dat gevoelige signalen op de printkaart verstoord worden door signalen op de chip en omgekeerd. Daarenboven kan de aanwezigheid van bijkomende diëlektrische lagen boven de ingebedde chip een invloed hebben op de voortplanting van signalen op de chip zelf.

Het algemeen gedrag van een meerlaagse microstrip transmissielijn, bestaande uit een combinatie van diëlektrische en halfgeleidende lagen, wordt verduidelijkt aan de hand van de parallelle-plaat benadering. Afhankelijk van de frequentie en de geleidbaarheid, treden verschillende voortplantingsmodes op. Bij hoge frequenties zal de halfgeleidende laag zich ofwel gedragen als een diëlektricum, ofwel, wanneer de indringdiepte kleiner wordt dan de dikte van de laag, als een geleidend grondvlak met hoge verliezen. Voor tussenliggende waarden van de geleidbaarheid en gematigde frequenties ontstaat een zogenaamde *trage-golf* mode die gekarakteriseerd wordt door een lage voortplantingssnelheid en geringe verliezen. Als gevolg van deze verschillende voortplantingsgebieden is het gedrag van het meerlagensubstraat sterk afhankelijk van de frequentie.

Er wordt bewust gekozen voor een eenvoudig, maar nauwkeurig model dat gemakkelijk toegepast kan worden aan de hand van analytische formules voor het ontwerp van microstrip lijnen. Het model is gebaseerd op twee gelijksoortige benaderingen die het meerlagensubstraat omvormen tot een gelijkwaardige enkelvoudige structuur. De complexe effectieve diëlektrische constante van de meerlaagse microstrip wordt berekend met behulp van een variationele methode. Hieruit wordt vervolgens de admittantie per lengte-eenheid afgeleid. Daarnaast resulteert het gebruik van complexe spiegelladingen in de berekening van een frequentieafhankelijke effectieve hoogte die gebruikt wordt voor het bepalen van de weerstand en de inductantie per lengte-eenheid. Het concept van het reduceren van het substraat tot een enkele laag en de introductie van de effectieve complexe hoogte maken het mogelijk om het gedrag van de meerlaagse microstrip op een consistente manier te beschrijven. Het principe van transversale resonantie dat aan de basis ligt van beide benaderingen, wordt echter wel minder nauwkeurig naarmate het aantal lagen toeneemt. Het grote voordeel ten opzichte van modellen die de volledige veldbeschrijving in rekening brengen, is dat dit model eenvoudig geïmplementeerd kan worden in hedendaagse hoogfrequente circuitsimulatoren.

Het vooropgestelde model wordt vergeleken met quasistatische elektromagnetische simulaties. Om de mogelijke beperkingen van het model bloot te leggen, worden een groot aantal geometrie- en materiaalparameters gesimu-

leerd. De capaciteit en de inductantie per lengte-eenheid worden door het model nauwkeurig voorspeld voor de gangbare dimensies van ingebedde componenten. Bij de verliezen treden er echter enkele afwijkingen op.

Tegelijkertijd werd een algemene methode ontwikkeld voor het bepalen van de diëlektrische constante en de verlieshoek van printkaartmaterialen. Hierbij wordt gebruik gemaakt van de ML-TRL kalibratietechniek om de propagatieconstante bepalen. Met behulp van analytisch uitdrukkingen worden vervolgens de materiaaleigenschappen afgeleid. De kostenbewuste volumeproductie van printkaarten brengt een aantal hoogfrequente beperkingen met zich mee, zoals de aanwezigheid van een soldeermasker en het feit dat de dikte van het baantje van dezelfde grootteorde wordt als de hoogte van het substraat. De ontwikkelde methode laat toe om de invloed van deze processtappen na te gaan en tijdens het ontwerp te compenseren.

Aan de hand van deze methode werd een specifieke testkaart ontworpen en vervaardigd, die de rechtstreekse extractie van de propagatieconstante van baantjes boven ingebedde chips mogelijk maakt. Na een grondige bestudering van de geometrische parameters en de materiaaleigenschappen van de testkaart worden de parameters per lengte-eenheid voor de microstrip boven de ingebedde chip berekend met het vooropgestelde model. Aan de hand van deze parameters wordt de propagatieconstante bepaald en vergeleken met de propagatieconstante afgeleid van de metingen. De totale nauwkeurigheid van het model in verhouding tot de metingen ligt binnen de 2 % voor de effectieve diëlektrische constante en rond 10 % voor de verliezen. Het model overschat de verliezen van de gemeten meerlaagse microstrip, maar is nauwkeuriger dan de simulaties in het voorspellen van de diëlektrische constante. Als laatste test worden de parameters per lengte-eenheid, gegeneerd door het model, gebruikt in een circuitsimulator voor het voorspellen van het gedrag van een baantje die over een chip heen loopt.

Het inbedden van chip in printkaarten heeft een aantal voordelen op het gebied van hoge frequenties ten opzichte van traditionele verpakkingstechnieken. De hoogfrequente karakterisering die in dit werk voorgesteld wordt zal bijdragen aan het ontketenen van het volledige hoogfrequente potentieel van deze nieuwe technologie.

English summary

Chip embedding is a three-dimensional packaging technology that offers an alternative to wire bonding and flip-chip interconnects. Two different categories of chip embedding technologies can be discerned. Fan-out wafer level packaging (WLP) enlarges the area available for interconnect routing on top of the die by embedding the chip in a polymer matrix. A more system level approach is offered by the direct embedding of active and passive components into a printed circuit board. This cost-effective solution removes the need for a package altogether. A first approach embeds the chips face-down in the core layers of the printed circuit board, either by the use of cavities or by punched openings in the prepreg. As an alternative, very thin dies are embedded in high density build-up layers of PCBs, using microvia technology to connect to the chip.

The embedding of the chip effectively creates a three-dimensional interconnection structure. In this way, not only the interconnection length between the chip and the board is minimized, but also the length of the signal path between different components. Terminating resistors or decoupling capacitors are placed directly above the appropriate pads of the chip and high-speed communication between two chips can be realized by placing the second chip on top of the embedded die. The vacant board space is used to optimize the routing of high-frequency signals, further reducing the discontinuities in the signal path. When the board space is limited, or when the contact pad is in the centre of the chip, high-speed signal lines may pass over the chip. To implement controlled impedance tracks in combination with embedded component layers, a detailed study of the influence of embedded chips on the impedance and loss of tracks running over and under the chips is performed. Dense metallization on the chip in combination with a redistribution layer can shield the influence of the layers below and act a virtual ground layer. A broadband model for these multilayer microstrips is introduced in this thesis and verified using simulations and measurements.

Other aspects of the high-frequency characterization of embedded components are the interconnection to the embedded die and the interference between signals on the embedded component and their surroundings. Due to the very low dielectric height above the chip, it is possible that critical signals on the

board are disturbed by signals on the chip and vice versa. Moreover, the presence of the additional dielectric layer above the embedded chip can have an influence on the propagation behaviour of on-chip interconnects.

The general behaviour of a multilayer microstrip transmission line is explained based on the parallel-plate approximation. The combination of dielectric and moderately conducting layers generates different propagation modes depending on frequency and conductivity. At high frequencies, the semiconducting layer will either behave as a dielectric or as a lossy ground plane when the skin depth becomes smaller than the thickness of the layer. For intermediate values of the conductivity and at moderate frequencies, a so called *slow-wave* mode occurs, characterized by a low propagation velocity and a small attenuation. As a result of these different propagation modes, the characteristics of the multilayer substrate are strongly frequency-dependent.

A simple and accurate model for the multilayer microstrip, which can be easily implemented using closed-form microstrip design formulas, is presented. The model is based on two similar approximations that reduce the multilayer substrate to an equivalent single-layer structure. The per-unit-length shunt impedance parameters are derived from the complex effective dielectric constant, which is obtained using a variational method. A complex image approach results in the calculation of a frequency-dependent effective height that can be used to determine the per-unit-length resistance and inductance. The concept of the single-layer reduction and the introduction of the effective complex height make it possible to accurately describe the behaviour of the multilayer microstrip in a concise way. The implementation can be readily expanded to more layers. In this case, however, the transverse resonance principle, which is the basis of both implementations, becomes less accurate. The big advantage over other, full-wave based models is that it can be used in existing microstrip design formulas and thus easily implemented in current RF circuit simulators.

The proposed model is compared to quasi-static electromagnetic simulations. A wide range of geometries and material parameters is included in the finite element method simulations to uncover possible limitations of the proposed model. For the dimensions common to embedded components, the per-unit-length capacitance and inductance are accurately predicted by the model, however, some discrepancies are present for the loss parameters.

In parallel, a general methodology for parameter extraction is developed to determine the dielectric constant and loss tangent of printed circuit board materials. The multiline TRL calibration technique is applied to extract the propagation constant, from which the material properties are derived using analytical formulas. The cost-conscious volume production of printed circuit boards introduces high-frequency limitations, such as the presence of a solder mask or a high plating thickness in combination with a thin substrate. The proposed method makes it possible to determine the influence of these process steps and to make corresponding adjustments at the design stage.

Using this method, a dedicated test vehicle is designed and manufactured, allowing the extraction of the propagation constant of traces running on top of embedded dies. After a thorough investigation of the geometrical and material parameters of the test vehicle, the per-unit-length RLGC parameters for the microstrips on top of the embedded die are calculated using the proposed model. From these parameters, the propagation constant is determined and compared to the propagation constant extracted from the measurements. The overall accuracy of the model in respect to the measurements is within 2 % for the effective dielectric constant and around 10 % for the loss. The model seems to overestimate the loss of the measured multilayer microstrip, but is more accurate than the simulations in predicting the effective dielectric constant. As a final test, the per-unit-length parameters generated by the model are used in a circuit simulator to successfully predict the behaviour of a track running across an embedded chip.

Embedding chips in printed circuit boards offers a number of high-frequency advantages over traditional packaging concepts. The high-frequency characterization presented in this work will help to unleash the full RF potential of this new technology.

List of Publications

The following journal papers have been published

- M. Cauwe and J. De Baets, "Broadband material parameter characterization for practical high-speed interconnects on printed circuit board," *IEEE Transactions on Advanced Packaging*, Vol. 31, pp. 649-656, 2008.

The following journal papers have been submitted for publication

- M. Cauwe and J. De Baets, "Propagation behaviour of multilayer microstrips applied to interconnects running near embedded integrated components," *IEEE Transactions on Microwave Theory and Techniques*.
- T. Demeester and M. Cauwe, "A reverse characterization algorithm of frequency-dependent substrates for microstrip interconnects," *IEEE Microwave and Wireless Components Letters*.

The following papers have been presented at international conferences

- A. Ostmann, D. Manessis, J. Stahr, M. Beesley, M. Cauwe and J. De Baets, "Industrial and technical aspects of chip embedding technology", *Proceedings of the 2nd Electronics System-Integration Technology Conference (ESTC)*, pp. 315-320, 2008.
- M. Cauwe and J. De Baets, "High-frequency modeling and measurements of tracks running on top of active components embedded in printed circuit boards," *Proceedings of the 16th European Microelectronics and Packaging Conference (EMPC)*, pp. 335-340, 2007.
- M. Cauwe, J. De Baets and A. Van Calster, "High-frequency characterization of embedded active components in printed circuit boards," *Proceedings of the 8th Electronics Packaging Technology Conference (EPTC)*, pp. 643-650, 2006.
- P. Van Daele, P. Geerinck, G. Van Steenberge, S. Van Put and M. Cauwe, "Laser ablation as an enabling technology for opto-boards," *Proceedings*

of the 53rd Electronic Components and Technology Conference (ECTC), pp. 1140-1146, 2003.

The following papers have been presented at national conferences

- M. Cauwe, "High-frequency characterization of embedded active components in printed circuit boards," Sixth FirW PhD Symposium, Faculty of Engineering, Ghent University, November 2005.

Contributions to technical publications

- M. Cauwe, W. Christiaens, J. Vanfleteren and J. De Baets, "Embedding active components as a 3D packaging solution," *Advancing Microelectronics*, pp. 15-19, May/June 2006.

Chapter 1

Introduction: Packaging technologies and high frequencies

Als de werkelijkheid er niet zou zijn,
zou de wereld er veel beter uit zien.
Theo Maasen

This doctoral research covers a new packaging technology which places active components inside the printed circuit board instead of on top. Besides the benefits in the area of cost saving, design freedom and thermal performance, this new technology offers some promising features for high-speed signals such as shorter signal paths and better impedance control. In order to position the embedding of active components in printed circuit boards in the world of advanced packaging, a short overview of current packaging solutions is presented in this chapter. After looking at the state of the art of three-dimensional package solutions, the focus is shifted to the benefits and challenges for high-frequency communication in advanced packaging.

1.1 3D packaging technologies overview

There are large differences in feature size and materials used in integrated circuits (ICs) and for printed circuit boards (PCBs). For this reason chips are packaged before they are assembled on a board. The function of a package is threefold. First of all, the package is needed to protect the fragile silicon from the outside world. Moisture, shocks, radiation, interference, etc. have to be

opposed by the package. A second important task of the package is to provide stress release between the die and the board. Thermomechanical effects cause strain and stress, which are not compatible with a rigid die. The final function of a package is to bridge the gap between the I/O pitch of the chip and the pitches used on the board, in order to create an electrical contact between the board and the chip.

Current electronic applications demand high-density, small-sized packages offering high speed and performance at low cost. All these aspects pose big challenges for assembly houses and printed circuit board manufacturers. Nowadays, two different target markets are emerging, each requiring different approaches and solutions. At one side, consumer electronics and mobile applications mainly focus on low cost. Although the functionality increases, the reliability becomes less of a priority due to shorter product cycles and today's consumer society. Situated at the other side of the spectrum, is the high-reliability market. Backbone infrastructure, military and medical applications need to be reliable and powerful. A common expectation in the telecommunications industry is a system availability of *five nines* (99.999%). This translates to only 5 minutes 15 seconds down time per year [1]. Advanced technology used to be driven by these specialized markets, but for the last couple of years, the constant urge for faster, more, smaller and cheaper in the consumer market has taken over the wheel.

Not only the product cycles, but also the consumer electronic products themselves have changed dramatically in recent years. When leaving on holiday a few years ago, one would take a digital camera to capture all those special moments and beautiful landscapes. A mobile phone would come in handy to contact the home front if necessary, while a portable personal information manager would store the information about the hotel and important dates of local activities. Of course a music player was brought along to provide some entertainment during travelling. Driving around for hours locating that small town in the mountains was avoided by installing a global positioning system (GPS) in your car. Nowadays, all these features are incorporated into a single device that fits inside our pocket!

An overview of different packaging technologies, from traditional to advanced 3D packaging, is outlined in the next sections. This overview is by no means an attempt to be complete, but rather focusses on common packages found in volume applications and printed circuit board assembly. Readers already familiar with the traditional packaging concepts, can immediately start with section 1.1.2. The outline of advanced packaging helps to understand the advantages and drawbacks of embedding active components in the build-up layers of printed circuit boards.

1.1.1 Traditional packaging technologies

During the 1980s assembled circuit boards looked quite similar to a modern city (Figure 1.1): large square buildings and round towers with wide roads in between. Electronic components were assembled in large packages with long leads that fitted into holes in the board. Students and hobbyists are most familiar with this so-called through-hole technology, since the large components are easy to handle, mount on the board and solder by hand. Passive components like resistors and capacitors consist of a cylindrical housing with two leads and can be placed perpendicular or parallel to the board. Integrated circuits are enclosed in dual-in-line packages (DIP), consisting of two rows of pins alongside a rectangular housing. The pitch of the leads is 2.5 mm with up to 64 leads (I/O count). In volume manufacturing, this technology is still very much alive today, due to the low cost or the fact that no other package is available, e.g. for components with low tolerance or large power dissipation. The through-hole connection is mechanically very strong and thus very reliable.

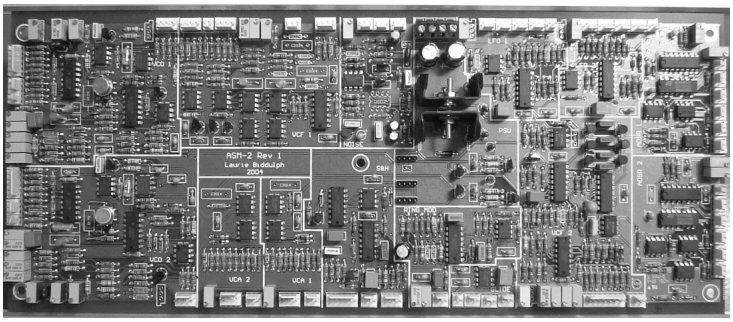
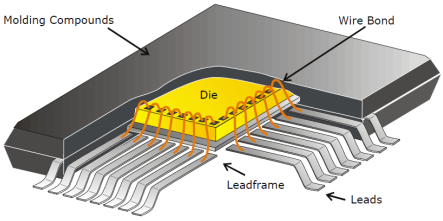


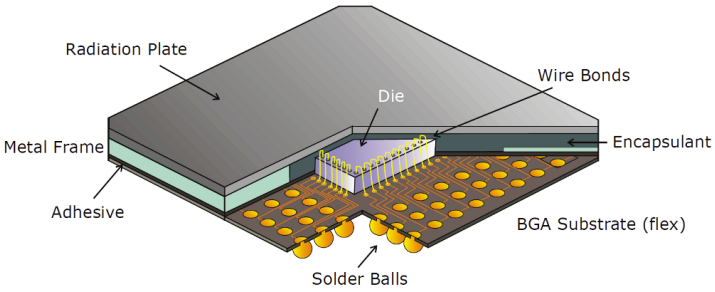
Figure 1.1: Printed circuit board with through-hole technology. Source: Elby Designs

The very large components and the large pitch put a constraint on the packaging density of the through-hole technology. This, in combination with the slow and challenging automatic placement, is one of the main reasons this technology has been replaced by surface-mount techniques (SMT). Surface-mount devices (SMD) do not require through-holes, but are soldered onto dedicated pads on a PCB. In order to realise a reliable solder joint, the solder pads must be large enough. The components do not have any leads in the case of passive components or very short and flat wing-like structures for active components. Recent adaptations also make it possible to use leadless connections or even solder balls for integrated circuits.

The main benefit of this technology is the highly automated and very fast assembly process. The finished printed circuit board is covered with a solder mask, leaving only the component mounting pads uncovered. To ensure a



(a) Leadframe package



(b) Structured substrate with solder balls

Figure 1.2: Schematic drawing of the different components of an electronic package

reliable contact after soldering, a surface finish is applied to the open copper pads. Solder paste, which consists of solder metal powder, flux and thixotropic agents, is deposited in highly controlled amounts using screen or stencil printing as well as dispensing techniques. The SMD components are then placed on their intended positions by an automated pick-and-place machine. Modern versions of these machines can place over 100.000 components per hour (IPC 9850). The tacky nature of the flux component in the paste keeps the components in place. When all the components are placed, the boards go to a reflow oven where the solder on the board is melted, forming a connection between the pads on the board and the pads or leads on the components. Next to the high-speed automatic placement, other advantages are the increased packaging density and the possibility of two-sided assembly. The large variety of components makes the process control more critical. The components themselves need to be compatible with the temperatures used during reflow (260 °C and more for lead-free soldering). All traditional packaging technologies that are described below, are based on this surface-mount technology.

In general, an electronic package consists of a carrier, onto which the chip is mounted, and pins that constitute the connections to the outside world. The

carrier can be a structured substrate (Figure 1.2(b)) or just a metallic frame (Figure 1.2(a)). Solder balls or metallic leads are the most common option for the pins of the package. The electronic connection from an integrated circuit to a printed circuit board (referred to as *board*) is split up in two parts: the interconnection between the chip and the package and the connection from the package to the board. The additional routing inside the package, if required, is considered here as part of the latter.

From die to package

The most widespread, and historically the most important, technology to connect the bond pads of an integrated circuit to the substrate or leadframe of the package is wire bonding. As the name implies, this approach uses very thin wires (25 µm diameter and less) to form the connection between die and package. Ball bonding is the most common type of wire bonding (Figure 1.3). At the tip of the bond tool, a spheric ball shape is formed. This ball is placed onto the bond pad of the chip, where the connection is made using thermal and ultrasonic energy (thermosonic bonding). The bond tool moves up and then sideways to the target location on the package, effectively making a loop. The second bond is formed by "smearing" the wire over the pad on the package, creating a wedge on the pad (wedge or stitch bond). The bond tool rises, breaking off the wire and leaving a small part of the wire sticking out of the tool (tail bond). This part is then used to form the ball by electronic flame-off, a sort of electric discharge.

Ball bonding is generally done using high-purity gold wires, but also alloy wires of less purity can be used in applications requiring high wire strength. Wedge bonding is an alternative technique, where aluminium wires are used to create a wedge bond at both ends of the wire. The aluminium eliminates the need for heating during the bond process (normally 150 °C to 240 °C, depending on the device). The wedge forming is directional and thus inherently slower. Recent developments also allow the use of copper wires for wire bonding [2].

The critical steps in the wire bonding process include achieving reliable bonds (first bond, second bond, and tail bond), maintaining desired loops, and positioning the bonds accurately. Throughput is also an important factor, since it affects the cost of the device. Technology drivers for wire bonding are fine pitch applications, multi-tiered ICs, and stacked dies. According to the ITRS 2007 roadmap [3], wire bonding fine pitch capability is currently at 35 µm in-line pitch.

One of the drawbacks of wire bonding is the placement requirement for the bond pads on the chip. The bond pads need to be placed on the periphery of the die and, in most cases, cannot be placed on top of active circuitry. The available space to place the bond pads is limited by the die size and thereby the

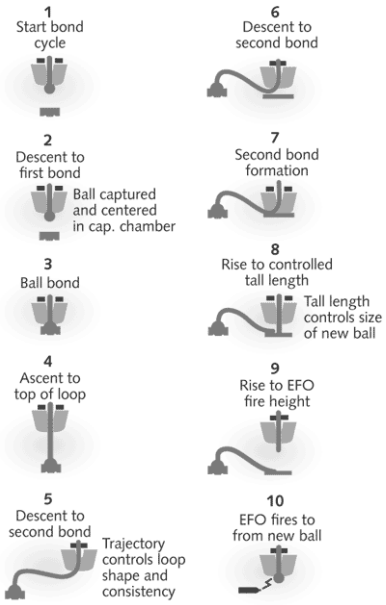


Figure 1.3: Process flow for ball bond wire bonding. Source: Advanced Packaging - Wire Bonding Tutorial

maximum number of input/output connections (I/Os) is also limited. A logical solution is to place multiple rows of pads, but this makes the wire bonding more challenging. These pad-limited dies, where the die size is determined by the edge space required for the bond pads, is one of the driving forces for an alternative electrical connection between the die and the package. Instead of placing the chip face-up on the substrate and using a wire to form the connection, the interconnection between the die and substrate is made through a conductive bump. The bumped die is then flipped over and placed face-down, with the bumps connecting to the substrate directly. This technology is called flip-chip interconnection and was originally developed by IBM for multi-chip applications on ceramic modules [4].

The assembly process for flip-chip interconnection is more complex than wire bonding, negating the possible time benefit over the sequential wire bonding process. The flip-chip connection is generally formed by using solder bumps. Before the solder can be applied to the pads on the die, an under bump metallization (UBM) process is performed at wafer level to remove the passivating oxide layer on the bond pad and to define the solder-wettable area. Solder may then be deposited over the UBM by evaporation, electroplating, or screen-printing. The solder bumped die is attached to a substrate by a solder reflow

process, very similar to the process used for surface-mount technology. Alternatives to the solder process are plated bumps using electroless nickel plating, stencil printing conductive adhesive, or stud bumping, where a soft gold bump is created. After the die is connected to the package substrate, a specially engineered epoxy is used to fill the area between the die and the substrate, surrounding the solder bumps. This underfill is designed to control the stress in the solder joints caused by the difference in thermal expansion between the silicon die and the substrate. Once cured, the underfill absorbs the stress, reducing the strain on the solder bumps, and thus greatly increasing the life time of the finished package.

Using flip-chip interconnections offers a number of possible advantages. Due to the shorter length of the interconnect (0.2 mm versus $1 - 5$ mm for bond wires), the inductance of the signal path is greatly reduced. This is a key factor in high-speed communication and switching devices and will be discussed in more detail in section 1.2. When the integrated circuit is specifically designed to use flip-chip interconnections, the entire surface of the die can be used to accommodate the bumps. This not only supports vastly larger numbers of interconnects on the same die size, but pad-limited dies can be reduced in size, saving silicon cost. Fine-pitch ICs with peripheral pads require a redistribution layer (RDL) to relocate the pads into an area array compatible with flip-chip interconnection. This redistribution layer consists of thin dielectric layers deposited over the wafer surface combined with copper tracks and pads. By eliminating the extra space needed to accommodate the wire bonds, the total package size can be reduced using flip-chip technology.

The minimum pitch that is compatible with today's flip-chip technology in volume manufacturing is 130 µm [3]. Traditional markets for flip-chip are high I/O count applications like microprocessors, graphics chips and game processors. Because of the higher mechanical strength and shock resistance, hand-held devices are also moving towards this technique. One of the determining factors in the choice between wire bonding and flip-chip is the cost. Due to the need for high-density routing on the substrate, flip-chip substrates today cost roughly twice as much as wire bond substrates. The crossover point for flip-chip used to be around 1000 I/Os [5], but rising gold prices have pushed that crossover point to a lower pin count of about 500 I/Os. Mobile and hand-held applications are typically in the 200-700 pin count range and are divided between (copper) wire bonding and an increasing flip-chip portion.

From package to board

The discussion of edge contacts versus area array for the interconnection between the die and the package is also relevant at the board level. After the die has been physically and electrically connected to a package substrate or

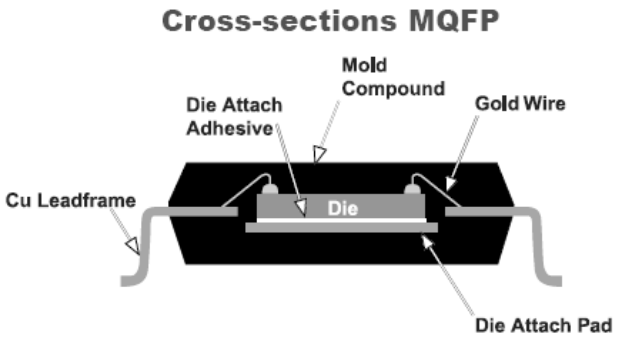


Figure 1.4: Cross-section view of a quad flat package. Source: Amkor Technologies

leadframe, these signals need to be routed out of the package and onto the board. The two main options here are peripheral leaded packages and area array packages. The different package categories presented below are distinguished by the type of connection between the package and the board, but can rely on both flip-chip or wire bonding for the interconnection between the die and the package.

Peripheral IC packages are an expansion of the classic dual-in-line package (DIP). The packages consist of a plastic body with leads emanating from two or four sides. Inside, there is a copper carrier onto which the semiconductor die is bonded using epoxy die bond material. The I/Os of the chip are connected to the metallic fingers of the leadframe by wire bonding. A plastic body is then moulded around the die and parts of the leads. Figure 1.4 shows a cross-section view of a quad flat package (QFP). Thanks to their low cost, peripheral leaded packages are still used for about 75% of the integrated circuits. The limitation of the I/O count with respect to the package body size, as discussed for wire bonding, is also relevant here. Due to the difference in coefficient of thermal expansion (CTE) between the board and the package, the maximum size of the body is limited by the stress that can be tolerated by the solder joint [6]. Limiting the body size of a peripheral leaded package automatically means limiting the number of I/Os. Lowering the lead pitch to increase the number of I/Os, requires finer lines on the printed circuit board, reducing yields and increasing board costs. The fine pitch also implies the use of very small leads, reducing the strength of both the lead itself and the solder joint. Special measures have to be taken during soldering to prevent bridging of the contacts [7]. Even with the finest QFP lead pitch of 0.3 mm, the number of connections is still limited to around 300 I/Os.

The outcome was again to move to an area array package type. Next to

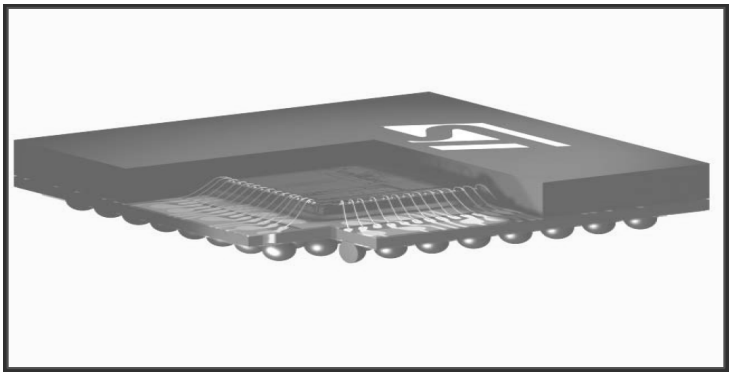


Figure 1.5: Three-dimensional view of a ball grid array package with wire bonding. Source: ST Microelectronics

initial solutions as the pin grid array (PGA) or the dedicated land grid array (LGA), the real workhorse of the area array packages is the ball grid array (BGA, Figure 1.5). This is a surface-mount package that utilizes an array of metal spheres or balls to provide an electrical interconnection. The principle is very similar to flip-chip solder bumps, although the pitch and ball size are much larger to improve the mechanical strength and reliability of the connection. The wider pitch simplifies the assembly process and reduces the requirements of the printed circuit board. Typical solder ball pitches for plastic BGAs (PBGA) are 1.27 mm, 1.0 mm and 0.8 mm. With a package size of up to 45 mm by 45 mm, the I/O count can reach 2500 and more. A peripheral package of the same size is limited to 480 I/Os.

The substrate of a BGA can be ceramic but is usually an organic laminate, similar to a printed circuit board. The die is attached to the top side by wire bonding or flip-chip in the case of a high I/O count. The chip and wires are then encapsulated either by cavity moulding with an epoxy moulding compound or by glob-topping with a liquid encapsulant. The laminated substrate can contain two to more than eight layers. Depending on the pitch at the chip side and the number of I/Os, a high-density interconnect (HDI) substrate may be required. The bottom side of the substrate is covered with pads where the solder balls are deposited. Solder ball placement starts by depositing flux on the pads of the substrate by screen printing. Pre-formed solder balls are then attached to the sticky flux by spreading the balls into holes of a metallic sheet that match the solder pads on the substrate, in a similar way to stencil printing. A final reflow step gives the solder ball their typical spherical shape. The package can be mounted to the printed circuit board at the same time as the other surface-mount components.

The main advantage of BGA as a packaging solution for integrated circuits

is the high interconnection density, reducing the package footprint on the board for a given numbers of I/Os. Another advantage offered by BGA packaging is the lower thermal resistance between the chip and the circuit board due to the possibility to use thermal vias within the substrate and thermal balls between the package and the board. These allow the heat generated by the device inside the BGA to spread to the board, preventing the overheating of the component. The shorter path between the die and the circuit board also leads to better electrical performance, since the short interconnection introduces less inductance and thus minimizes the distortion of signals in high-speed applications. Power planes may also be incorporated into the substrates to further reduce power and ground inductance.

The primary drawbacks of the ball grid array are stiffness of the solder balls and the tracking of defects. Flexural stresses from the circuit board can easily be transmitted to the package and its joints. The inability of the solder balls to flex compared to leads can cause potential reliability issues. In addition, once the BGA has been soldered onto the board, the balls and solder joints underneath the package are difficult to inspect. Non-destructive evaluation of the complete package requires the use of X-ray inspection equipment.

Chip-scale packaging

The next step in the search for higher packaging density is to scale down the ratio of the area of the package compared to the die size. QFP and BGA are several times bigger than the actual die because of space required for leads or large solder balls and for routing in the substrate. Reducing the size of the package can free up a large amount of board space, which was one of the main drivers for the development of chip-scale packages (CSP). The name does not really point at a specific packaging technology, but is defined by Joint Electron Device Engineering Council (JEDEC) as a surface-mountable package not more than 20% larger than the die size.

There are dozens of different designs of chip-scale packages available, which basically all consist of an interposer onto which the die is attached and of wire bond or flip-chip interconnections between the die and the interposer. This interposer can be a rigid substrate (ceramic or organic), a flexible substrate (usually polyimide), a leadframe or just a number of redistribution layers directly on the wafer. The last category are the so-called wafer level chip-scale packages (WL-CSP). The advantages offered by chip-scale packages include smaller size, lesser weight, lower overall production costs, and improvement in electrical performance.

CSPs with rigid or flexible substrates use a ball grid array to connect to the board but, because of the limited package size, the pitch of the solder ball needs to be reduced. These finer pitch versions are often referred to as fine-pitch ball

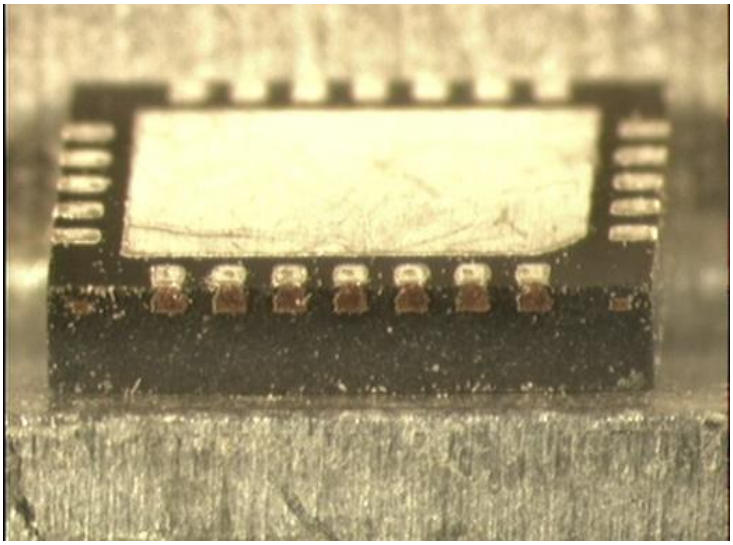


Figure 1.6: A quad flat no-lead package with exposed pad

grid array (FBGA) or micro-BGA. Pitches down to 0.4 mm, with 250 µm ball pads, are posing new problems for printed circuit board manufacturing and assembly. The fine line and spaces needed to route the signals to and from the CSP can only be obtained by using dedicated build-up layer technology, consisting of thin resin layers ($50 - 150\,\mu m$) in combination with blind microvias of 150 µm diameter. In assembly, the small pitch, and the associated ball size, is reducing yield and reliability. Smaller balls put higher constraints on planarity and introduce thermomechanical issues similar to flip-chip technology, requiring extra measures such as underfill and thus increasing cost [8].

The most widely used leadframe CSP is undoubtedly the quad flat no-lead (QFN) package. The QFN is a leadless package, where the leads are replaced by solder pads at the edge of the package (Figure 1.6). The major benefit of this package is the substantial reduction in overall cost, since there is no need for expensive substrates or advanced PCB processing to accommodate fine-pitch solder ball arrays. The lack of leads results in a direct signal path from the top of the die to the backside of the solder connect pad, offering improved electrical performance compared to the convoluted path through various vias and multiple metal layers on the substrate of a FBGA package. The backside of the die attach pad (DAP), onto which the die is placed, can be exposed and connected down to the DAP land on the motherboard. This results in a direct thermal pad to the active area on the die. Reliability issues after reflow are countered by strict PCB design rules and tight control of the soldering process.

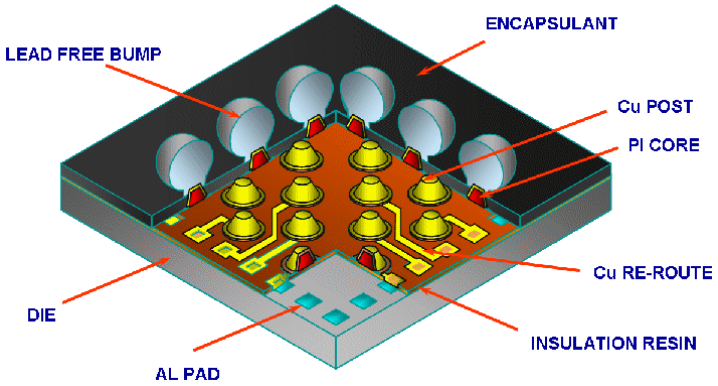


Figure 1.7: Three-dimensional view of a wafer level chip-scale package. Source: Fujikura/TI

QFNs are available in sizes from $3 - 9\,\text{mm}$ and with 2 to 100 I/Os, providing a direct replacement for peripheral leaded packages.

The majority of the process steps for wafer level packaging (WLP) are, as the name implies, carried out at wafer level. These packages are made before the wafer is diced, therefore their size cannot be larger than that of the die. The technology process is similar to the application of redistribution layers, with extra attention to mechanical stress relief for the ball attachment and encapsulation of the die (Figure 1.7). These WL-CSPs contain no stiff interposer that can absorb the thermomechanical stress between the package and the board. Due to difference in coefficient of thermal expansion (CTE) between the printed circuit board ($17\,\text{ppm}/^\circ\text{C}$) and the silicon chip ($4\,\text{ppm}/^\circ\text{C}$), the maximum die size is limited. The use of underfill can be prevented by using a large I/O pitch of 0.5 mm, restricting wafer level packages to integrated circuits with relatively low pin count [9]. WLP technology is ideal for portable communications and related applications that require a low cost packaging solution with small form factor and improved signal propagation characteristics.

Smaller BGA pitches and advances in high-density PCB manufacturing opened the door for the final step in the package miniaturization. Direct chip attach (DCA) removes the need for any package by directly attaching the chip to the board using flip-chip technology. The biggest disadvantage is the need for known-good die (KGD). When the chip is packaged, it can be tested before assembly and replaced if faulty, loosing only the cost of the packaging. By attaching the chips directly to the board, it is necessary to know in advance if the die itself is fully functional, since otherwise the complete board has to be scrapped. After curing of the underfill, it is not possible any more to repair

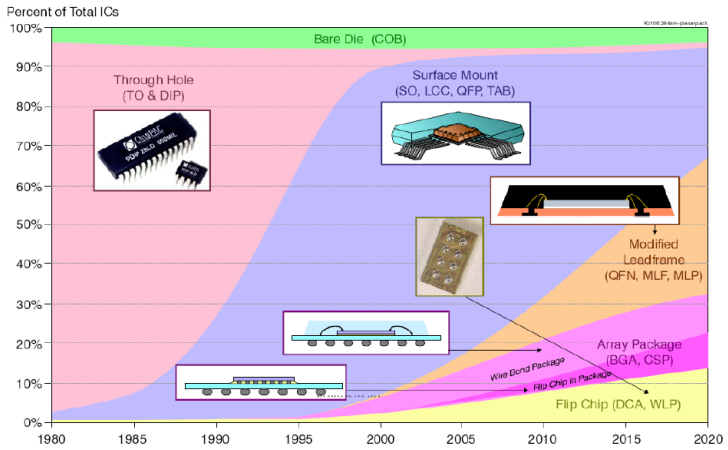


Figure 1.8: Market forecast for different package categories. Source: Prismark 2009

or replace the package. A chip-on-board technology using wire bonding also exists, but is not compatible with the surface-mount assembly process and thus rarely used.

Overview of the packaging market

Looking at a market forecast by Prismark in 2009 (Figure 1.8), it is clear that leadframe packages will remain the dominant package type in the coming years. The cost benefit of the leadless peripheral package causes a strong growth in market share, which will be sustained in the next decade. The growth rate of area array and wafer level packages is lower, but nonetheless the market penetration of these packages is steadily increasing. The dominance of the leaded packages will be replaced by a more diverse package spectrum, offering optimal solutions for each application area.

1.1.2 Need for advanced packaging

Assembly and packaging is the final process step of IC manufacturing, transforming semiconductor devices into functional products for system integration. The package provides electrical connections for signal transmission, power input, and voltage control and plays an important role in thermal dissipation and the physical protection of the chip. Today, assembly and packaging is a limiting factor in both cost and performance for electronic systems. The key driver for the growth of the electronic industry has been the continuous reduction in cost

per function. Historically, the preferred approach to sustain this growth was the scaling of the wafer fabrication processes and improvements in design. The cost of packaging has not kept pace with the cost reduction in wafer fabrication, so the packaging cost often exceeds the silicon IC fabrication cost. Advances in metal layer processing for ICs and ecological legislation are causing a further increase in the cost of packaging, making cost reduction even more challenging. Lead-free solder materials and low-k dielectrics are more costly than the materials they replace. Next to higher processing temperatures, portable consumer electronics are exposed to a wider range of temperatures during everyday use, and thus require new, more expensive, substrate and interconnect technology.

The size and weight reduction offered by advanced packaging makes it possible to implement more semiconductor functions on a given board space or reduce the board space for a given set of functions. This paves the way for the integration of different applications into a single device. Such a trend has become very obvious in the mobile phone market, where cell phones incorporate music and video players, cameras, wireless internet connection, GPS and so on. The reduced size also enables more design freedom to create innovative new form factors and styling.

The ability of hand-held devices to store calendar information, play games, access the internet, watch streaming video and listen to streaming audio, and perform other functions that were once only handled by computers, not only requires faster logic chips, but also strongly increases the memory requirements both in performance as in capacity. All cellular and application code, as well as user data, for a basic 2^{nd} generation phone could be stored into some 1664 megabits of NOR Flash and some 28 megabits working memory (SRAM) for the baseband CPU and DSP processors [10]. High-speed protocols used on 3G phones require memory performance and capacity far beyond the requirements of the previous generation. The smart phone operation system itself can take up some tens of megabytes of storage and working memory space, augmented with up to 16 gigabytes of multimedia data storage.

System-on-chip (SoC) and system-in-package (SiP) technologies have the potential for continued improvement in performance, power, cost and size at the system level without relying upon conventional CMOS scaling alone. The SoC implementation realizes the entire system on silicon, offering the highest level of miniaturization, performance and cost reduction in volume manufacturing. The very complex design process, however, leads to high development costs and long time to market. With the current short product cycles, this technology does not offer the flexibility needed for consumer electronics.

System-in-package technology has rapidly evolved from a dedicated technology used in a narrow set of applications to a high-volume solution with a wide ranging impact on electronics markets. As the name implies, SiP is *a combination of multiple active electronic components of different functionality,*

assembled in a single unit, which provides multiple functions associated with a system or sub-system (definition courtesy of the ITRS committee). The broadest adoption of SiP to date has been for stacked memory with logic devices and small modules for mobile phones applications.

The production price of a SiP module is higher than a comparable system-on-chip, but the time to market is much shorter (3 to 6 months instead of 12 to 24 months) and the development effort is also significantly reduced. SiP allows for the use of different chip technologies (RF, analog, optical, MEMS) as well as common, low cost components. Individual chips can be replaced or redesigned without the need for a complete redesign of the system. The supply chain for the different types of chips, together with the complex assembly, are possible drawbacks. Design tools that integrate the system design from the chip level up to the board interconnection are still not common, compared to the automated CAD tools that are available for SoC design.

Incorporating several chips in one packages introduces thermal issues, due to different cooling requirements. High-power chips need a direct thermal path to a heat sink, with as low as possible thermal resistance. Removing the generated heat requires a large volume, counteracting the size reduction of the package. Placing chips with different thermal requirements close to each other can cause additional local self-heating effects. For instance, if a low power memory is placed very close to a high heat dissipating processor, the temperature range that the memory will be subjected to will be higher regardless of its own power dissipation. Aside from the pure thermal challenges of cooling the SiP, the increased heat flux has a direct impact on the reliability of the interconnects. As the components run hotter, the stress fluctuations are higher when the device is power cycled, degrading the reliability.

Looking at the inside of the second generation iPhone (Figure1.9), several types of advanced packaging technologies are revealed. Both the baseband processor and the UMTS transceiver combine two chips into one BGA package. The Samsung application processor is provided in a package-on-package (PoP) stacked configuration with 128 megabytes of DRAM. The wireless LAN controller is a system-on-chip configuration, the GPS receiver is delivered in a chip-scale package, and finally the quad-band power amplifier is a system-in-package. This example shows that the correct package has to be chosen for each application, in order to offer the best compromise between cost and performance.

More features at reduced cost will continue to drive the search for innovative and cost-effective packaging solutions. The performance needs of consumer electronics have reached levels that where only required in dedicated applications a few years ago. Finding a suitable technology for volume markets remains the main challenge for future package research. Advanced packaging technologies can help to overcome this bottleneck for electronic component

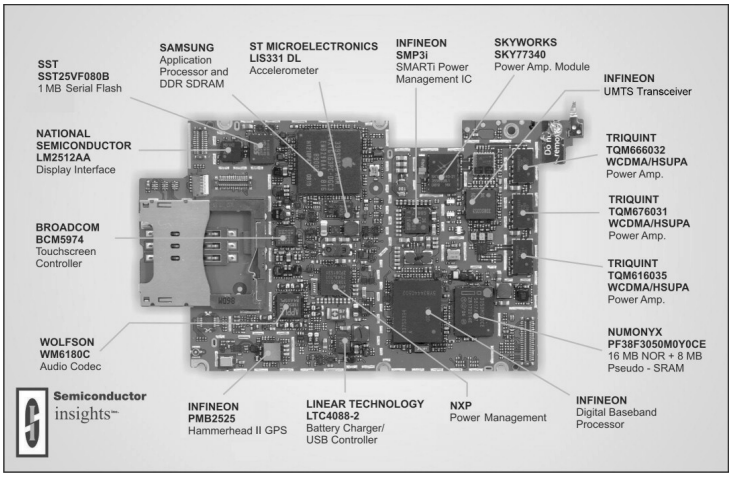


Figure 1.9: Printed circuit board for Apple iPhone 3G. source: Semiconductor Insights

manufacturing.

1.1.3 3D packaging state of the art

The latest trend in advanced packaging is the use of the third dimension to further increase the packaging density. 3D packaging offers short signal paths, smaller form factor and the possibility of cost reduction by integrating several chips in one package. Most of the challenges regarding materials, manufacturing infrastructure and reliability are similar to the single die packages, and thus research efforts and results can be adopted in both directions.

To minimize the total height of the package, 3D packaging technologies often require wafer thinning. Wafer thinning down to 50 um thickness consists of a two-step wafer back grinding process followed by a polishing step. Stress introduced in the thin-film layers of the semiconductor circuit causes the thin wafers to curl up into a roll if left unsupported, rendering further processing with conventional equipment impossible.

The first implementation of 3D packaging on production level was bare die stacking, which is sometimes referred to as stacked-die CSP. Thinned dies are placed on top of each other and connections to the board or between chips are made by wire bonding. This process has the advantage of using existing capabilities and offers a high degree of freedom in connecting chips to substrates. As the number of dies increases, wire bonding processes become more and more complex and the longer wires cause an increase in inductance and signal

delay. Samsung, Hynix, and Elpida, three major memory suppliers, all demonstrated the ability of stacking up to 20 memory chips in a single 1.4 mm-thick package, using dies thinned down to 25 µm (Figure 1.10). Current production implementations are limited to stacks of 5 to 7 dies.

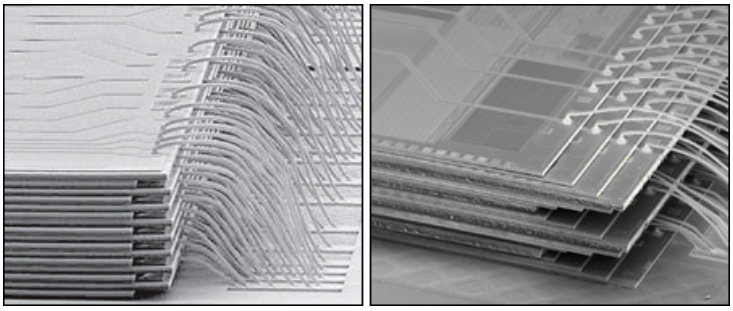


Figure 1.10: Microscopic view of the stacking of memory chips by Samsung Electronics (left) and Hynix (right). source: Korea Times

The majority of stacked die package applications today use wire bond interconnects on leadframes and rigid or flexible substrates. Hybrid wire bond/flip-chip connections slowly start to emerge. Interconnecting stacked dies offers big challenges for the wire bonding equipment. Wire bond loop control is very critical for die stacks of three chips and more. Due to the stacking of various die sizes, bonding on thin overhanging dies and forward and reverse bonding with very low loop height are a necessity.

The problem of escaping I/Os from stacked die is that all the signals have to be wired out to the edges of the stacked chips and are then connected down the side of the stack to the next level of interconnection. So despite saving weight and volume, current technologies do not shorten the interconnection length nor enhance the performance in most cases. 3DIC technology with through-silicon vias (TSV) can help solve these issues [11]. These vias present a direct connection through the thinned wafer and offer the shortest possible signal connection between chips. The vias are formed by etching (before or after thinning) or laser drilling of thinned silicon. The biggest processing challenge is the filling of the high aspect ratio vias, which can be done by plating or conductive paste. The small diameter vias require a very high placement accuracy during stacking and attachment methods that can cope with the stress inside the wafer after via formation. TSVs are believed to be the gateway for high-volume bare-die stacking in the coming years [12].

Apart from the technological challenges of bare die stacking, the main research drivers for the development of other stacking approaches are the requirement for known-good dies (KGD) for high product yield and the fact that the chips can only come from a single source. By stacking finished packages in

stead of bare dies, the components can be tested before stacking, and thus the KGD issue is overcome. Chips from different suppliers and even different chip technologies can be combined. Drawbacks of this package-on-package (PoP) technology are a higher package profile compared to bare die stacking and the complex infrastructure needed for package stacking. Digital still cameras and mobile devices are the main applications for PoP packaging technology. Typically the logic parts belong to the bottom package and the top package is the memory. This has the advantage, when needed, that the memory density can be varied by changing the top package.

Warpage is one of the main reliability issues with package-on-package, due to the different CTE of the materials involved. The stacking of the packages is performed by placing the bottom package on the motherboard and the following packages on top. The connections between the packages as well as the connections to the boards are realised in a single reflow step. Warpage of the bottom package during reflow causes gaps between solder balls of bottom package and PCB solder lands [13]. Package design and material selection are critical for reducing warpage, and thus thermomechanical simulation and modelling are required for each PoP construction.

Chip embedding as packaging solution

Today, 3D system integration consists of the combination of active and passive devices, especially silicon ICs, into a package structure which is then connected to a board. An alternative approach is the embedding of passive and/or active devices directly into a board or substrate. Advantages of the latter are the reduced product volume, extremely short signal paths for improved RF performance, the possibility of build-in EMI shielding, almost no routing restrictions and a high-volume manufacturing process, resulting in a cost-effective solution.

A multitude of chip embedding approaches are available in different stages of development, ranging from research prototypes to mass production ready. The concept of embedding active components as an alternative packaging method was already introduced in 1975 in a patent application by Tokyo Shibaura Electric Co., Ltd in Japan [14]. For this first implementation, the chips are partially embedded *"in a metal substrate where a dielectric layer is overlaid on the substrate with the semiconductor chips projected through windows of the dielectric layer"*.

Two different categories of chip embedding technologies can be discerned. The first set of technologies follows a packaging approach where singulated dies are embedded in a single- or multi-chip module serving as a drop-in replacement for traditional packages. The difference compared to standard WL-CSPs is the possibility of using a fanout design for the reconfiguration of the chip pads. A more flexible and advanced approach targets the embedding of chips directly

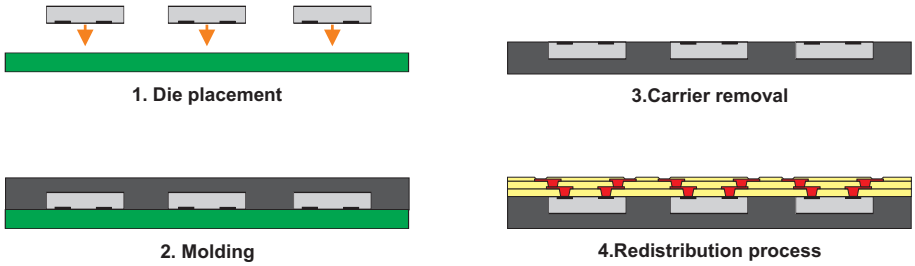


Figure 1.11: Process flow for fanout chip embedding

into the printed circuit board, removing the need for a separate package or traditional mounting technique. These system-in-board (SiB) modules offer a totally new concept of component packaging, but also create new challenges for design tools, manufacturing flow and supply chain.

The fanout solution offers the next step in wafer level chip-scale packaging as the die size no longer determines the package size. By slightly enlarging the routing area, components with higher I/O count can now also take advantage of the reduced cost and improved electrical properties of chip-scale packaging. Despite the larger package size, the signal path remains very short since the signals do not need to pass through a substrate. The larger package footprint can also help to overcome thermomechanical issues through the use of larger pitches and thus larger solder balls.

A number of technologies are available from different companies and research institutes, which all follow a similar process flow (Figure 1.11). The singulated dies are placed with the active side face-down on a carrier with a standard assembly pick and place tool. The dies are then encapsulated with an epoxy moulding compound. After curing the epoxy and possibly grinding down the backside of the mould, the encapsulated dies are released from the carrier. The epoxy panel with the dies can be shaped like a normal wafer, so the subsequent redistribution process can be performed on standard silicon manufacturing equipment. This redistribution process is a combination of depositing insulating and metal layers. The dielectric layers can be laminated or spin coated, while the vias are usually drilled by laser. The copper metallization layers are deposited by electroplating techniques and then structured. Thanks to the use of very fine lines and spacings (25 µm L/S currently, 15 µm under development) and low via pitch (130 µm, with 40 µm in development), the size of high I/O count packages can be significantly reduced. Different types of active and passive components can be placed together on the carrier and are encapsulated to form a functional system-in-package.

One of the first to introduce the fanout embedding technique was General Electric with their *Chip First Build-Up* or *Embedded Chip Build-Up* [15, 16].

The latest version of this process flow uses flexible polyimide film as the carrier, which also serves as the first build-up layer on top of the chip. The backside of the die can be exposed to connect to a heat sink. Infineon calls their technology *Embedded Wafer Level Ball Grid Array (eWLB)* [17] and have recently announced a cooperation with ST Microelectronics and STATS ChipPAC, a leader in advanced 3D packaging solutions, to further develop the technology for volume production. Freescale already demonstrated a Radio-in-Package module, implementing their *Redistribution Chip Package (RCP)* packaging technology [18]. The module integrates a baseband processor, memory, RF and PA modules, and power management components into a package the size of a postal stamp (18 mm by 20 mm).

In 2001, the bumpless build-up layer (BBUL) package was introduced by Intel to anticipate future issues with electric performance and to reduce the thermomechanical stress on the sensitive low-k dielectrics [19]. Due to the slower increase of processor frequencies and the transition to multicore designs, Intel has postponed the introduction of BBUL into mass production until future processor generations. Instead of using reconfigured wafers, this technique places the tested die into a punched cavity on a laminated HDI substrate. The embedding of the dies in the panel may be done with moulding or dispensed encapsulation material.

The Institute of Microelectronics at the Agency for Science, Technology and Research (A*STAR) in Singapore developed a package technology where copper pillars of different height are deposited on the pads of various chips [20]. The height of the pillars depends on the position of the chip in the stack, in such a way that the top of the pillars is at the same height after stacking. The dies covered with a mould compound and after grinding, the copper pillars are exposed and connected to solder pads using a redistribution technique. The proposed package combines the benefits of wafer level packaging, fanout interconnects and 3D integration without the use of any interposers.

The *Chip-Last Embedded Active* approach from the Packaging Research Centre at the Georgia Institute of Technology is distinguished from previous technologies in that chips are embedded *after* build-up layer processes are completed [21]. Main benefits are the reworkability of defective chips by the use of reworkable interconnects, such as solder, and better process yield since no complex processing after chip embedding is needed. Since the backside of the thinned chip is directly accessible, the thermal management is also improved. The cavities are formed by various processes, based on current microvia formation techniques. This enables the use of existing equipment with well-known materials and established parameters. The methods used for cavity formation are photo-imaging using photosensitive dielectric materials, plasma etching, laser drilling and dielectric cavity layer lamination, which uses dry film with pre-cut cavity openings. After cavity formation, the chips are flip-chipped into

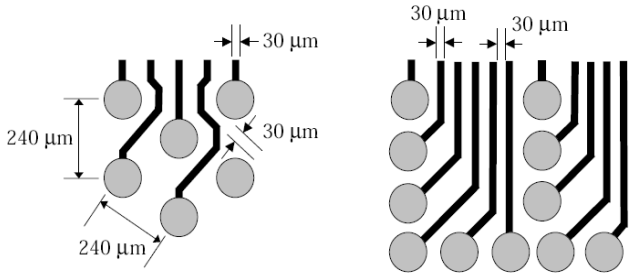


Figure 1.12: Escape routing advantages of embedded components. Flip-chip interconnections require a regular pattern to allow sufficient flow of the underfill (left). When using embedded components, the placement of the die-package interconnect can be arbitrary (right). This poses less restriction on the escape routing

the cavities using fine-pitch solder interconnect, followed by filling with underfill and adhesive materials. One major disadvantage of this technology is that it is not possible to use the area above the chip for routing or stacking additional chips. The use of flip-chip technology to connect the die to the substrate also inherits the drawbacks of this technology regarding underfill and routability (Figure 1.12).

The fanout packaging technologies still end up with a package that has to be mounted to the printed circuit board and thus face similar drawbacks of classical packages, such as solder interconnect reliability and thermomechanical issues. A cost-effective solution is to skip the packaging step altogether and directly embed the chip into the printed circuit board. This frees up the board area above the chip, removes some of the routing restrictions caused by area array interconnects (see Figure 1.12) and reduces cost.

All mayor PCB manufacturers are either developing their own solution for embedding active components or are licensing one of the technologies from the research institutes. The use of well established processes and equipment, slightly adapted to the requirements for chip embedding, makes these technologies very cost-effective and inherently robust. The cost saving comes from the parallel processing of large panels and the reduction of board area and number of layers. However, the yield of the embedding process, and all PCB related processes after embedding, is very critical for the cost. A failure in one of these steps, results in scrapping of the board with embedded components, losing the cost of the board, the processing and the die inside the board. The yield of the different processing steps needs to be well above 95 % for cost-effective volume

production.

Panasonic developed a new 3D module using embedded passive and actives to reduce cost and size with increased functionality [22]. The proposed technology combines printed circuit board layers with a composite layer containing the embedded components. Two PCB substrates are assembled with passive and active components and matching cavities are made in the composite layer. Interconnections through this composite layer are formed by filling inner via holes with conductive paste. The whole structure is pressed together, embedding the components and interconnecting the two PCB substrates in one step. Current issues are related to solder mounting the passive components, underfilling the active components and the reliability of the inner via structure. Another drawback of the technology is the large pitch of the inner vias (400 µm) and the large distance required between via and chip (1.2 mm), possibly negating the advantage of shorter wiring length through embedding.

The chip embedding of Dai Nippon Printing [23] is based on the Buried Bump Interconnection Technology (B2IT), originally developed by Toshiba [24]. Silver cones are stencil printed onto a copper foil and then the hardened cones are pressed through a prepreg sheet. By placing an additional copper layer on top and laminating the whole stack, high-density layers with build-in connections are formed. Several of these layers can be combined to make up a multilayer board, but it is also possible to mix the technology with standard core layers with through-holes or build-up layers with microvia technology. By placing SMD components on one of the B2IT layers and creating matching openings in the layers above, passive components can be embedded inside the stack-up. A similar approach is used to embed active components, where the thinned chips are attached to the lower layer using flip-chip technology.

Almost ten years ago, Casio developed a WL-CSP for use in lightweight mobile devices. Instead of relying on copper bumps and solder balls, this technology uses copper pillars of 90 µm to 150 µm height encapsulated in an epoxy resin. The top of the copper pillars are dipped in solder to attach the package to the board. The use of copper pillars in combination with the encapsulation material ensures a better CTE matching between the package and the board and acts as a thermomechanical stress release layer. This technology uses less solder, can achieve finer pitches and the copper has better thermal and electrical conductivity than solder. In 2002, a cooperation was started with the Japanese board manufacturer CMK Corporation to embed this wafer level package into a printed circuit board [25]. The WLP is mounted face-up onto an intermediate printed circuit board. The embedding of the package is achieved by lamination of pre-cut glass reinforced prepreg layers in combination with a thin RCC layer on top of the WLP. Microvias to the copper posts of the WLP are laser drilled and metallized. Figure 1.13 provides a cross-sectional view of the *embedded wafer level package (eWLP)* after positioning of the solder balls.

Since October 2006, production applications include system-in-package modules for a GPS watch and a digital TV tuner modules. More recently, a 0.4 mm thick power amplifier module was realised, including an embedded DC power management IC, which was placed face-down inside a cavity in the 100 µm core layer [26].

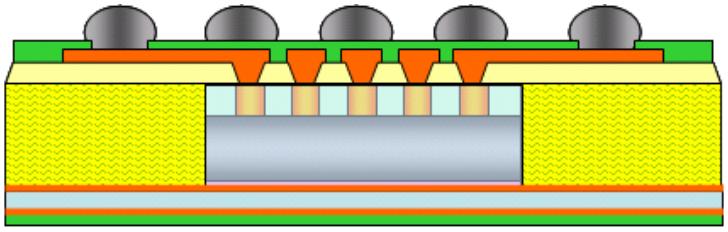


Figure 1.13: Cross-sectional view of the embedded WLP from Casio and CMK

The first *Integrated Module Board* generation was developed at the Helsinki University of Technology in 1999 [27]. The original process did not use vacuum lamination, but chips were embedded using a moulding compound and the contacts to the chip were opened by grinding down the epoxy mould. A second IMB generation (IMB-C) was presented in 2000 and later industrialized by Imbera Electronics Oy [28]. In this version of the technology, the IC components are embedded inside a cavity that is manufactured into a PCB core layer. The interconnection between the IC and PCB is done using build-up layers and plated microvias. The minimal PCB structure for the second generation IMB-C is a double-sided core layer with a build-up layer on each side. The embedding was a complex process, that required extra processing steps as well as build-up materials. To simplify the process flow and reduce the cost, a third generation (IMB-R) of the technology was introduced [29].

For the third generation process (Figure 1.14), alignment marks and via openings are laser drilled into a copper foil. The chips are placed onto the copper foil using adhesive that is printed or dispensed on the foil. The placement can be done with high-speed surface-mount equipment or high-accuracy flip-chip bonding machines for small pitch applications. The alignment of the components is performed by lining up the chip pads to the via openings in the copper foil. To manufacture the core layer, prepreg sheets with matching openings and a second copper foil are piled on top of the lower foil. During vacuum lamination the resin liquefies, effectively embedding the chips. The core laminate with the components inside can be further processed using common PCB patterning processes. A CO_2 laser drilling step removes any remaining epoxy or adhesive from the via openings. The microvias can now be metallized and the copper conductors are manufactured using subtractive etching or pattern plating. Because the IMB core layer can be used like a standard PCB core

layer, various multilayer configurations can be manufactured.

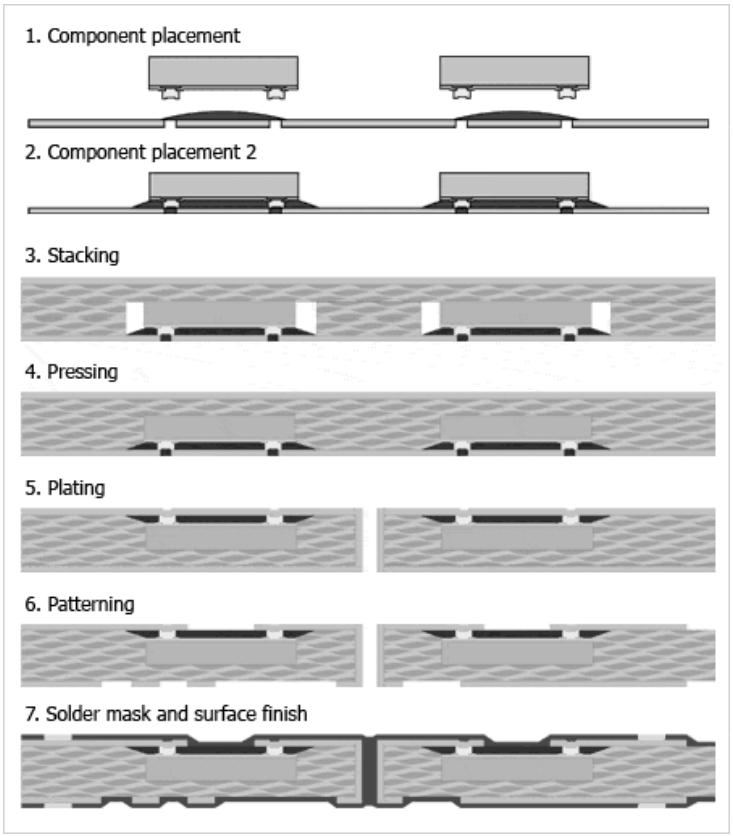


Figure 1.14: Third generation process flow for the Imbera Integrated Module Board

Next to the simple and cost-effective process flow, another big advantage is the single alignment step. By fabricating the via openings and the alignment marks in one step, the components can be aligned very precisely with regards to the vias and thus the wiring on the board. More details on alignment issues can be found in section 2.3.7.

In 2002, the Technical University of Berlin proposed an alternative to the embedding of thick chips in the core layer of a printed circuit board [30]. The Chip in Polymer (CIP) technology embeds very thin dies (around 50 µm) in the build-up layers of PCBs, taking advantage of the higher routing density and minimizing the additional height required for the package. The first implementation of this technology was aimed at the realisation of stackable chip-scale

packages and used a liquid photo-dielectric to cover the chips. The technology was further developed by using vacuum lamination for the embedding of the chips and printed circuit board technology for the generation of interconnections. A European consortium, the HIDING DIES project, was formed to transform the chip embedding principle into a production technology.

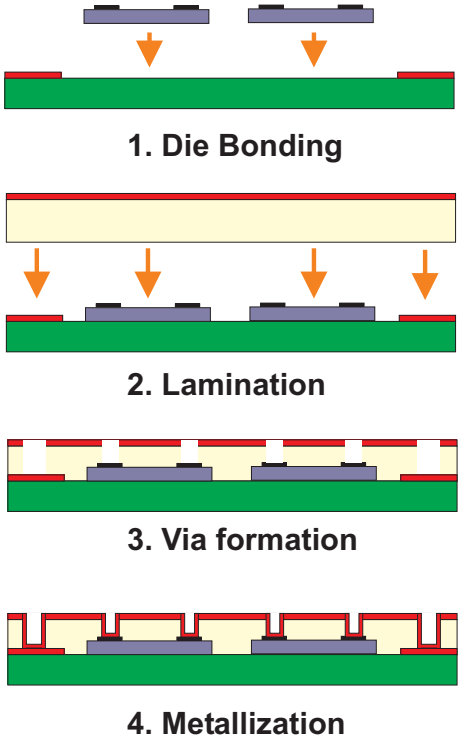


Figure 1.15: Process flow for embedding active components in the build-up layers of a printed circuit board

A detailed explanation of the technology platform can be found in chapter 2. Figure 1.15 gives a schematic overview of the process flow. The thinned chips are placed on dedicated die bonding positions on a core substrate, using local die bonding fiducials to maximize the placement accuracy. The adhesive layer below the chip needs to be as thin as possible with excellent planarity. The actual embedding of the chips into the PCB structure occurs in the vacuum lamination step. The core substrate with the die bonded chips is covered from both sides with a resin coated copper (RCC) build-up layer. The laser drilling of vias to the bond pads of embedded chips is comparable to the formation of microvias on PCBs. In the first step the copper of the RCC above the pads of the chip is removed. Then the dielectric is removed by a laser until

the Cu bump is reached. The final process step is the metallization, using a combination of electroless and galvanic plating, and structuring of the copper by wet etching.

A Japanese PCB house, Shinko Electric Industries, has published some information on their embedding trials in 2003 [31], but it is not clear if there are any volume production activities. Shinko embeds ultra thin chips (20 µm thickness) in the build-up layers of a printed circuit board. The chips can be placed either face-up or flip-chipped and are embedded by vacuum laminations without special cavities. The boards are finished using laser drilled microvias and high-density structuring.

The research efforts which are put in all these different approaches show that the embedding of active components as advanced packaging technology is gaining momentum. Apart from providing significant size and performance improvement compared to existing manufacturing solutions, a robust process with consistent high yield levels is necessary to gain wide industry acceptance. The technology should be easily accessible for the customers, without significant change in their supply chain, product structure, or design flow. At this moment, the fanout solutions are the first candidates for volume production, due to their low cost, in-house processing and clear supply chain. For direct embedding in PCBs, current efforts for volume production focus on the embedding of chips in the core layers of the PCB. This process is most suited for manufacturing on large panels and thus the most cost-efficient. To avoid alignment issues on large panels, the chips still require an additional redistribution layer. The experiences gained from these first steps should trigger chip suppliers to adapt chip embedding as a valuable packaging option, further reducing the overall cost and optimizing the technology to reach the highest packaging density.

1.2 High-frequency characteristics of 3D packaging

This section gives an overview of the effect of advanced packaging methods on the high-frequency performance. Miniaturization and increased density result in a shorter signal path and therefore reduce the values of parasitic parameters. New technologies introduce new challenges, requiring a detailed study of the high-frequency behaviour of these packaging techniques.

1.2.1 Benefits

Improved high-frequency characteristics can be obtained in two different ways. The first approach is miniaturization. By making the signal path as short as possible, compared to the effective wavelength of the signal, the negative

effects of the interconnection can be minimized. An alternative way is to try to optimize the high-frequency behaviour of the interconnection by avoiding perturbations in the propagation of the electromagnetic fields. An example of the first approach is minimizing the length of bond wires, reducing the total inductance of the interconnection proportional to the decrease in length. Using controlled impedance tracks on package substrates is an illustration of the second technique. 3D packaging concepts often combine shorter signal paths with increased design freedom for track routing and optimal placement of terminating resistors and decoupling capacitors.

Before discussing the advantages of advanced packaging techniques over traditional technologies as wire bonding and flip-chip interconnect, a quantitative evaluation of the high-frequency performance of a number of packaging techniques is presented.

High-frequency performance of advanced packages

Since package leads or solder balls are very short connections, they can be described using a lumped element model, even at high frequencies [32]. This approach assumes that the delay time of the interconnect is smaller than the period of the signal. Each interconnect is described using a resistance R, an inductance L and a capacitance C. Since the series reactance at high frequencies is usually a lot higher than the resistance, the interconnection can be seen as a LC delay line. The impedance of the connection is determined by the ratio of the inductance and the capacitance.

$$Z_l = \sqrt{\frac{L_l}{C_l}} \tag{1.1}$$

This impedance is used as a first order approximation to model the reflection caused by the package lead. When a transmission line with characteristic impedance Z_C is connected to the package, the value of Z_l compared to Z_C determines the behaviour of the signal. When the lead impedance is smaller than the characteristic impedance of the line, the capacitance required to balance the inductance of the lead with respect to the characteristic impedance of the line is smaller than the capacitance of the lead. This excess capacitance of the lead can be easily calculated.

$$C_N = \frac{L_l}{Z_C^2} \tag{1.2}$$

$$C_{ex} = C_l - C_N = C_l - \frac{L_l}{Z_C^2} \tag{1.3}$$

In a similar way, an excess inductance can be defined. When the characteristic impedance of the lead is larger than the characteristic impedance of the connected line, the inductance needed to balance the capacitance is smaller than the inductance of the lead.

$$L_N = C_l Z_C^2 \tag{1.4}$$
$$L_{ex} = L_l - L_N = L_l - C_l Z_C^2 \tag{1.5}$$

This simple model allows for the interconnect to be modelled as a short section of transmission line with characteristic impedance Z_C, delay L_l/Z_C or $C_l Z_C$, and a shunt excess capacitance or a series excess inductance respectively in the middle of the line. The first-order model can be applied to any transition that is electrically short compared to the rise time of the signal. The delay of the lead can be estimated by the formula below and the rise time of the signal should be at least three times larger.

$$\tau_l = \sqrt{L_l C_l} \tag{1.6}$$

Amkor Technologies, one of the leading package houses, supplies the resistance, inductance and capacitance values of their packages based on simulations at 100 MHz. The derived electrical parameters are published in the data sheet for the respective packages. In Table 1.1, the values are shown for two types of quad flat packages (the standard MQFP and the low profile LQFP), for a small outline integrated circuit (SOIC) package, which is a SMD version of the dual-in-line package, and for a chip scale package using flip-chip technology (fcCSP).

Table 1.1: Electrical parameters for different package types

	SOIC	MQFP	LQFP	fcCSP
number of pins	28	44	48	64
size (mm^2)	8x18	10x10	7x7	8x8
inductance (nH)	1.42-5.05	1.46-1.66	0.96-1.11	0.26-2.16
capacitance (pF)	0.345-1.09	0.32-0.34	0.2-0.225	0.18-0.38
resistance (mΩ)	8.04-28.7	17.0-19.8	12.0-13.8	7-53.9

The numbers are given for the longest and the shortest connection and do *not* include bond wire or flip-chip bump parasitics. Notice how the shortest leads on the SOIC package are comparable to QFP, but the longest leads have very high inductance. The CSP offers very low values for the inductance and the capacitance, but due to the redistribution of the chip pads, some inter-

connections can become quite long and have a negative impact on the high-frequency performance (see section 1.2.2). To visualize the difference between these values, each package was simulated using a π-model with the resistance and inductance in series and half the shunt capacitance on each side. A pulse with a rise time of 50 ps was used to drive the connection, which corresponds with a bandwidth of 10 GHz. The simulations were performed using the Spectre RF SPICE simulator that is part of the Cadence design suite. Figure 1.16 shows the results of the simulations. Both the CSP and the LQFP have no problem following the fast rising slopes and only introduce a small delay. The MQFP and the SOIC package deteriorate the rise time of the pulse, causing a significant delay in the decision point of the logic.

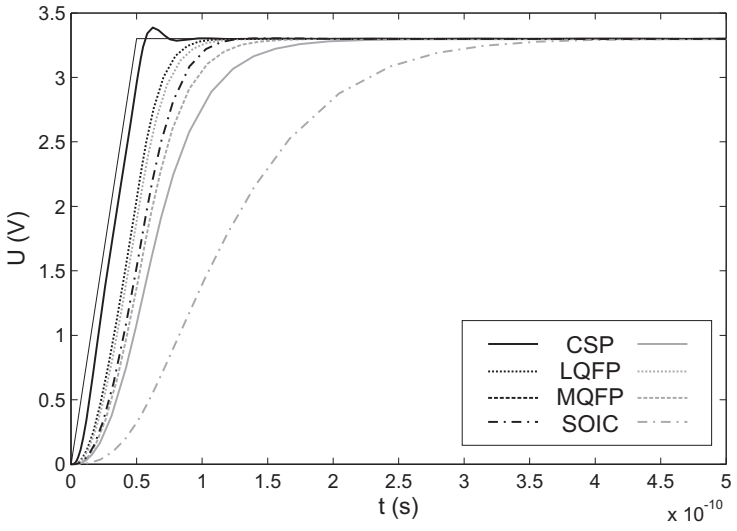


Figure 1.16: Step responses for the package types of table 1.1

Table 1.2 shows the excess inductance or capacitance for the shortest connections of the packages when connected by a 50 Ω line . Notice that all the leaded packages show an excess inductance, caused by the longer length of the interconnect, but the chip scale package actually shows an excess capacitance. This can also be seen from the overshoot in the step response. Calculating the values for the longest SOIC lead, the excess inductance is about 2.3 nH. The lead delay, however, is 74.2 ps, so the accuracy for the lumped element model for our 50 ps rise time is limited. Overall, it is clear that the reduction in package inductance leads to improved high-frequency performance.

Minimizing the excess inductance or capacitance is the idea behind a technique called discontinuity cancellation. This technique was successfully applied to enlarge the bandwidth of a PBGA package from 20 GHz to over 40 GHz [33].

Table 1.2: Excess inductance or capacitance for different package types

	L_l (nH)	C_l (pF)	Z_l (Ω)	τ_l (ps)	L_{ex} (nH)	C_{ex} (pF)
SOIC	1.42	0.345	64.16	22.1	0.56	
MQFP	1.46	0.320	67.55	21.6	0.66	
LQFP	0.96	0.200	69.28	13.9	0.46	
CSP	0.26	0.180	38.01	6.9		0.076

The plastic ball grid array package uses wire bonding to connect the chips pads to the substrate. The signal is routed to teardrop shaped ball pads through the substrate using vias. The bond wire introduces excess inductance, while the ball pad increase the capacitance. The inductance of the bond wire is minimized by placing the contact pads on the substrate closer to the chip and thus decreasing the length of the wire. The reference plane underneath the solder pads on the substrate was cut away and the antipad of the via, the space between the ring of the via and the reference plane, was enlarged. The size of the cut-out and the antipad were tuned to remove all excess capacitance. These simple measures sufficed to double the bandwidth of the package at virtually no cost.

Next to the improved high-frequency input/output signal integrity, advanced packaging technologies offer a higher quality of the power delivery, avoiding timing violations and increasing component lifetime. Braunisch et al. studied the electrical performance of the bumpless build-up layer packaging using transient electromagnetic simulations for the core power delivery problem [34]. A lumped-element model of a power delivery structure is introduced to describe the influence of on-die current swings on the die voltage. Figure 1.17 shows a schematic of the model, where V_0 is the DC supply voltage, $v(t)$ is the voltage across the on-die decoupling capacitance C_d and $i(t)$ is the on-die current. The package is modelled using the inductance L_{p1} and the on-package decoupling capacitance C_p, with its associated parasitic inductance L_{p2}. The traces between the package and the power supply are represented by the inductance L_s.

When switching between low and full power states, large average current swings occur on the die. During the first few nanoseconds following the current step, the relatively large inductance L_s effectively isolates the power supply from the rest of the circuit ($L_s \to \infty$), combining L_{p1} and L_{p2} into the loop inductance L_p of the package. The current step causes the voltage $v(t)$ to oscillate, which is referred to in the paper as "*drooping*" of the die voltage. Assuming C_p is much larger than C_d, the magnitude of the first voltage minimum

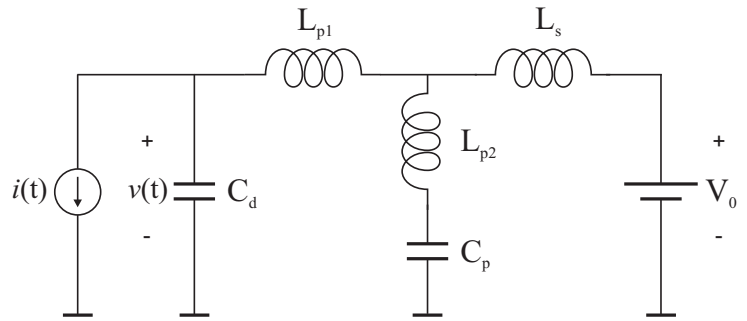


Figure 1.17: Lumped-element model for a power delivery circuit [34]

is given by

$$V_1 = \Delta I \sqrt{\frac{L_p}{C_d}} \tag{1.7}$$

Drooping of the voltages on power planes below their minimum allowed values may occur if decoupling is not adequate.

Transient EM simulations of the power delivery circuitry are performed to validate the assumptions of the lumped-element model. A flip-chip package with a six layer substrate using plated through-holes is compared to an equivalent BBUL package with three layers. Details of the simulation setup can be found in the paper [34]. The simulations reveal that the natural frequencies of the resonant switching noise waveforms are well below 200 MHz and the corresponding wavelengths are much larger than the lateral package dimensions. A lumped-element representation of the package is thus acceptable. The dependence of the voltage drooping on the package loop inductance in (1.7) is also confirmed. The BBUL package reduces the magnitude of the first voltage droop by 25%, caused by the decrease of the effective loop inductance by 61%. In fact, for a thin pacakge such as BBUL, the loop inductance is almost equal to the parasitic inductance of the decoupling capacitor on the package. The reduction of the voltage swing may allow the usage of a smaller on-package decoupling capacitance with a lower associated parasitic inductance. The simulations, however, show that oscillations in the next level of decoupling determine a second droop, depending on the amount of C_p, similar to the dependence of V_1 to C_d. In conclusion, the inductance of the chip-to-board connection is mostly determined by the length of the connection and advanced packaging methods can strongly reduce this length.

High-frequency advantages of 3D packaging concepts

According to the advanced packaging report of TechSearch International, over 85 % of all current integrated circuits are packaged using wire bond technology. The only areas where flip-chip is dominant are pad-limited designs or where high-frequency performance is crucial. From a high-frequency viewpoint, a bond wire is a very bad interconnection. There is no clearly defined ground reference, as in the case of microstrip or striplines, and the interconnections are relatively long ($1 - 5\,\mathrm{mm}$). Due to the lack of ground reference, the capacitance of the interconnection is quite small. In comparison however, the inductance of the interconnection is quite large. On average, 70 % - 90 % of the power path inductance is concentrated in the bond wire for PBGA packages, and 30 % - 70 % of the power path inductance is concentrated in the bond wire for leadframe packages [35]. The high-frequency drawbacks of wire bond technology will now be discussed in more detail.

Bond wire interconnects can be analysed as a lossy transmission line whose characteristic impedance is determined by the series inductance and shunt capacitance per unit length of the transmission line. To minimize reflections for high-frequency signals, a matched impedance along the entire signal path is desired. Due to their large inductance, conventional bond wire configurations exhibit high characteristic impedance and thus have a strong influence on the signal integrity. By placing multiple bond wires in parallel, the series inductance can be strongly reduced, but the spacing of the wires needs to be finely tuned to optimize the results [36].

Crosstalk between adjacent bond wires can be a major issue. Bond wires are typically quite long, run parallel to their neighbour and are placed close together due to small pitches on the die. When there are insufficient ground wires or when the ground wires are placed far apart, the return current for the high-speed signals needs to travel over a long distance, creating a large loop inductance. If two signals share the same ground reference wire, their corresponding signal-return loops will overlap, causing a large inductive coupling between the signals. This can be avoided by placing ground wires next to each high-speed signal wire.

In the case of stacked die packages, the coupling and crosstalk effects between wire bonds are even more critical. To minimize the total height of the package, or to stack as many components into a given height, the individual dies are thinned down further and further ($25\,\mu\mathrm{m}$ and below, see Figure 1.10). As a result, the various layers of wire bonds that connect the dies to the substrate, are getting closer to each other. This is a new coupling scheme not seen for single die packaging. The wires for the top dies may also become longer, causing these problems to appear at lower frequencies.

Some of these drawbacks of bond wires can be minimized by taking into

account a few basic design rules during the layout of the chip and the package. Due to the higher pitch of the bond fingers on the substrate or leadframe, the bond wires for the bond pads in the corners of the chip will be longer than those at the centre. By placing the bond pads for the critical signals in the middle of the edge of the chip, the length of the bond wire can be reduced dramatically. To minimize crosstalk and loop inductance, reference ground wires should be placed as close to the signal wire as possible. The length of the return path can be further reduced by using segmented power or ground rings close to the die.

All these drawbacks show that wire bonding can be a serious bottleneck for high-performance integrated circuits. A solution is to sacrifice cost for increased performance by using flip-chip technology to connect the die to the substrate. Replacing the long bond wires with solder balls greatly reduces the inductance in the signal path. Since the solder balls can be placed across the entire surface of the die, the power signals can be brought directly to the location on the die where they are needed, in stead of first being routed to the edge of the die. This results in a further reduction of the inductance and consequently reduces the simultaneous switching noise[1].

A generic, low pin count flip-chip ball grid array (FCBGA) package uses a laminate-based substrate, generally consisting of two to six layers. Mechanically drilled through-hole vias are used to connect to different layers of the substrate. Through-hole vias occupy valuable routing space on the carrier, so this type of substrate is limited to low pin count applications. In applications demanding greater functionality with higher pin counts, the substrate consists of a combination of core and build-up layers (6 to 14 metal layers). The vias through the build-up layers are created using laser drilling techniques, making it possible to apply blind and buried vias. Fanning out the connections from the flip-chip bumps to the BGA solder ball can be very complex. The substrate may require multiple high-density interconnect layers on top of the two or four layer core. The signal path from the chip to the board can become relatively long, especially when the substrate contains large through-holes. The large signal-return loop can introduce problems with crosstalk and ground bounce (figure 1.18).

The performance of the BGA package can be further improved by eliminating the plated through-holes from the substrate. This can be achieved by embedding the chip into the substrate, minimizing the interconnection length between the chip and the solder balls. To ensure a reliable connection to the

[1] When multiple output drivers on a chip switch simultaneously, they induce a voltage drop in the package power distribution, momentarily raising the ground voltage within the device relative to the system ground. This phenomena is commonly referred to as *ground bounce*. The resulting ground bounce voltage is proportional to the inductance present between the component and the power supply, causing slower switching speeds at the output drivers that will result in jitter and timing problems.

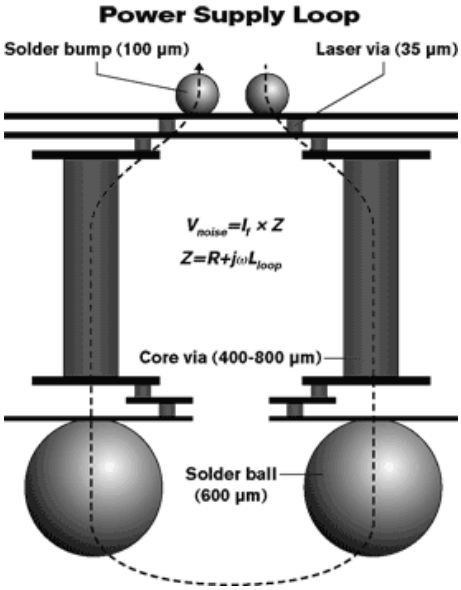


Figure 1.18: Signal-return loop for a high pin count BGA package. The main portion of the signal path inductance is caused by the plated through-holes

board, BGA balls with large diameter are needed. The interconnection length can thus be reduced further, by embedding the chip directly into the board, removing the need for solder balls completely.

The embedding of the chip effectively creates a three dimensional interconnection structure. Not only the interconnection length between the chip and the board is minimized in this way, but also the length of the signal path between different components. Terminating resistors or decoupling capacitors can be placed directly above the appropriate pads of the chip (Figure 1.19). High-speed communication between two chips can be realised by placing the second chip on top of the embedded die. The vacant board space can be used to optimize the routing of high-frequency signals, further reducing the discontinuities in the signal path.

Increasing packaging density and the placement of multiple chips into a single module or package, in combination with the fast rising and falling edges of high-speed electronic signals can cause problems with electromagnetic interference (EMI). To minimize the electromagnetic interference between components and to protect sensitive RF circuitry, some form of shielding is required. This can be a dedicated metal enclosure placed over the package or a conductive layer that is build into the housing of the chip. An example of the latter is the use of conductive sprays or electroplating on the plastic package material. As

an alternative, the polymer for the package moulding can be mixed with conducting (carbon) fibres. Embedding sensitive components inside the substrate or board offers a natural solution to these EMI problems. The copper layers on top of the die can be used as upper shielding, while a via cage can be formed to completely isolate the chip form the surroundings. This shielding method can be very cost-effective since the application and structuring of the layers is required anyway.

1.2.2 Challenges

New packaging concepts often show great promise for increased performance in a number of application areas. 3D packaging technologies offer short signal paths and increased flexibility for routing, but as a result of the complex geometries and their inherent three-dimensional nature, this improved high-frequency behaviour is not always readily available. A number of difficulties common to these advanced packaging techniques are discussed in this section. At the end, some specific challenges related to chip embedding are considered.

Whether it is the build-up layer of a wafer level package or the complicated stacking arrangement for PoP configurations, new developments introduce new restraints for optimal high-frequency signal transmission: the presence of redistribution layers, new materials or existing materials in new locations, specific location of the chip(s) inside the package, controlled impedance restrictions and the availability of electrical modelling tools. Each of these limitations needs to be overcome in order to utilize the full RF capabilities of the new technology.

By design, most chips are intended to be wire bonded and the bond pads are placed along the edge of the chip, with pitches down to 35 µm. When these dies are flip-chipped or embedded, a redistribution layer (RDL) is required to change the location of the peripheral die pads to an area array-type distribution with a more relaxed pitch (above 150 µm). This redistribution layer can extend the interconnection length of critical signals, increasing the risk of switching noise and crosstalk. In extreme cases, I/O signals are first routed to the peripheral pads of the chip and then again redistributed to bumps elsewhere on the die surface. Improper design can even result in reduced performance compared to wire bonding.

In [37], a comparison between the high-frequency characteristics of a bond wire and a flip-chip connection, including the redistribution layer, is performed. The simulations include lumped-element parameter extraction, reflection and insertion loss, and crosstalk. Looking at the extracted RLC values (Table 1.3), the combination of the flip-chip bump, the via and the attached RDL line shows parasitics that are similar to those of the bond wire. However, when calculating the excess inductance in relation to a 50 Ω transmission line, the flip-chip interconnection is better matched. This is confirmed in the paper by simulating the

Table 1.3: Lumped-element parameters for wire bond versus flip-chip [37]. Note the high resistance for the flip-chip interconnection due to the thin metal on the redistribution layer

	R_l (mΩ)	L_l (nH)	C_l (pF)	Z_l (Ω)	L_{ex} (nH)
Bond wire	138	3.40	0.210	127.3	2.875
FC with RDL	549	2.23	0.838	51.59	0.135

reflection. The lines on the redistribution layer can be designed using a controlled impedance. This impedance control across the entire interconnection is a major advantage of the flip-chip interconnection.

3D packaging technologies in general and chip embedding in particular introduce new materials or apply existing materials in areas where they are not expected. For example, the die attach layer of an embedded die has an influence on the propagation of signals on tracks running underneath or on top of the chip. These materials are until now not characterised for high frequencies and information as the dielectric constant or loss factor may be hard to come by. Measuring the material parameters can be challenging, since most of these materials are only available in their final form and not as bare material.

Electrical detuning of on-chip interconnects and other integrated structures is a known effect in flip-chip mounting of high-frequency components [38]. When the carrier substrate surface comes near to the chip surface, the propagation characteristics of the circuit on the chip can be altered. While this is a reasonable concern for GaAs microstrip based circuits, and to a smaller extent for coplanar waveguides on GaAs, CMOS based integrated circuits using thin-film microstrip lines are considerably less influenced due to the very short distance between the signal line and the ground plane [39]. Embedding or chip stacking places the chip in a different surrounding compared to traditional packaging concepts. As a result, the presence of, for example, an additional dielectric layer above the embedded chip will undoubtedly have an influence on the characteristic impedance and propagation of on-chip interconnects. A similar effect can be caused by metal structures, dummy or not, that are placed close to RF signal lines. Whether these disturbances lead to timing issues or not, will depend on the timing budget of the chip and the interconnect length.

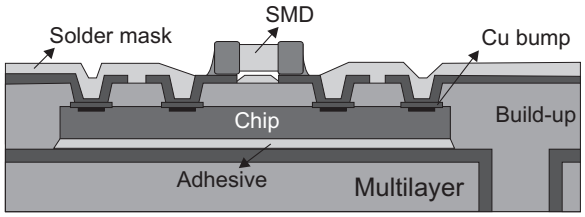
Not only the impedance of on-chip interconnects is affected by the placement of the chip, but signals on the chip can couple to lines on the board or substrate or even to other chips in the package. These interferences are only apparent in the final layout of the package and are thus hard to predict.

Because of the layout of the chip or limited routing space on the substrate, it is not always possible to minimize the interconnection length. In order to optimize the high-frequency signal transmission, reflections along the signal

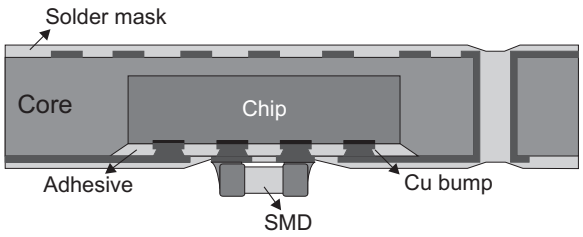
path need to be avoided where possible. This can be done by matching the impedance of the chip-to-board connection to the transmission line carrying the high-speed signal on the board. Controlled impedance designs are a common occurrence in printed circuit boards and therefore the PCB suppliers have established design rules and verification methods such as integrating time domain reflectometer (TDR) test coupons on the panel for verification of trace impedances. However, package level interconnects typically feature compact design rules with traces as narrow as 25 μm in HDI substrates and 55 μm in low cost organic substrates and are thus more susceptibility to manufacturing tolerances. The lack of experience of substrate suppliers with controlled impedance packaging and the design rules for package interconnects make impedance control difficult at the package level [40]. Another drawback of the decreasing line width and spacing on high-density substrates is the increasing resistive loss, both at DC as at high frequencies. For long lines, the effect on signal integrity can be larger than the effects caused by mismatch.

Electrical modelling of system-in-package during the design phase is very critical. Until recently, RF modules were designed using circuit simulators in the frequency domain for analog applications or in the time domain for digital systems. Board interconnections were included by employing planar transmission line models and packages were modelled using lumped-element parameters (SPICE or IBIS models). However, the traditional approach of modelling separated parts of the signal path is hitting its limit, due to high-density routing and non-standard geometries such as chip stacking or embedded components. For demanding RF applications, the chip, substrate and board need to be co-designed, in order to optimise the performance and avoid complicated workarounds at one level to compensate for inadequate design on another level. This also means that the entire system needs to be simulated with one tool, offering a good balance between accuracy and simulation time.

A wide variety of commercial electromagnetic extraction tools is available, ranging from 2D solutions for planar structures to full 3D solutions with a broad offering of materials and modelling capabilities. Due to the inherent 3D nature of SiP packaging, electric modelling of these systems requires 3D electromagnetic simulations. The 3D simulator can be a (quasi-)static solver, valid for lengths much shorter than the wavelength of the signal. Static field simulators solve Poissons equation for the electric field $\mathbf{E}$ and the magnetic field $\mathbf{H}$ separately to examine capacitive and inductive effects. The static solvers are very practical because they can rapidly extract low-frequency lumped element models for complex 3D packages including package routing and coupling between bond wires. At the other side, it is also possible to use full-wave 3D field solvers, solving the wave equation derived from Maxwells equations with $\mathbf{E}$ and $\mathbf{H}$ fully coupled and valid up to very high frequencies. The output of these simulators are often S-parameters, which are difficult to interpret correctly and



(a) Embedding in a build-up layer



(b) Embedding in the core layer

Figure 1.19: Schematic drawing of two methods for chip embedding in printed circuit boards

are not compatible with some SPICE circuit simulators.

1.3 High-frequency challenges for the component embedding technologies

The high-frequency properties of embedded active components are the main focus of this doctoral study. Modelling the high-frequency characteristics of embedded components makes it possible to identify the limitations of the technology in comparison with competing approaches, as well as aid the designer in implementing the technology in an optimal way. The combination of the embedded component with the surrounding printed circuit board faces the following challenges:

- Propagation behaviour of tracks running on top of, underneath or near embedded components
- Behaviour of interconnections to embedded components
- Interference between signals on embedded active components and structures on the printed circuit boards

- Integration with embedded passive components for power plane decoupling or line termination

Little research has been performed in this area so far, due to the relatively new technology and the atypical geometries that are involved. The influence of the cavities required for the chip-last embedding from Georgia Tech is investigated in [41] through measurements and simulations. Since the presence of the chip is not taken into account, the behaviour of the microstrips inside the cavity is similar to those on the top level. In [42], the same authors investigate the coupling noise between power and ground caused by the openings in the planes required for the cavity. These issues are specific to the chip-last embedding, because there is no metallization above the chip with this technology. Other publications do consider the effect of the silicon chip, but are more targeted towards wafer level packaging [43, 44]. For the embedding of chips in printed circuit boards, the interconnection between the chip and the board is investigated for the Integrated Module Board [45] and for the Chip in Polymer technology [46]. The latter is applied to an automotive radar sensor at 77 GHz and reveals performance similar to wire bonding. However, further optimization of the technology should improve the performance. Ohshima et al. [47] describe the design of a package with embedded chip and compares the performance to a FCBGA package, but also fails to incorporated the semi-conductive behaviour of the chip.

1.3.1 Propagation behaviour of board interconnects running near embedded integrated components

Since the chip is incorporated in the board, the space above the chip becomes available for routing. When the board space is limited, or when the contact pad is in the centre of the chip, high-speed signal lines may pass over the chip. To implement controlled impedance tracks in combination with embedded component layers, a detailed study of the influence of embedded chips on the impedance and loss of tracks running over and under the chips is required. In addition, dense metallization on the chip in combination with a redistribution layer can shield the influence of the layers below and act as a virtual ground layer.

Tracks running over embedded components can be described as multilayer microstrips, consisting of dielectric and moderately conducting layers, with different propagation modes depending on frequency and conductivity. When the conductivity of the semiconductor (σ) is low compared to the dielectric displacement ($\omega\epsilon_0\epsilon_r$), all layers will behave as dielectrics. The propagation mode is appropriately called *dielectric mode*. When the conductivity is very high, the magnetic field will fail to penetrate the conductive layer, which will start acting as a lossy ground plane. This mode is called the *skin effect mode*.

For intermediate values of the conductivity and at moderate frequencies, the magnetic field will penetrate the entire substrate. The electric field, however, will be concentrated in the dielectric layer(s). This decoupling of the electric and magnetic field leads to a significant decrease in propagation velocity, hence the name: *slow-wave mode*. The specific transition frequencies depend on the material and geometrical parameters of the multilayer sandwich.

As a result of these different propagation regions, the high-frequency behaviour of the multilayer substrates is strongly dependent on frequency. To quantify this behaviour, a broadband model of the multilayer microstrip is introduced in chapter 3 and compared to quasi-static electromagnetic simulations. A dedicated test vehicle that allows for the direct extraction of the propagation constant of these multilayer microstrips is manufactured and used to verify the model (Chapter 5).

The remaining challenges will be discussed shortly in the following sections.

1.3.2 Investigation of the interconnection to the chip

The interconnection between the chip and the outside world can have a substantial influence on the high-frequency performance of a package. Bond wires, for example, exhibit excessive inductance due to their relatively long length and the lack of good ground reference. For critical RF applications, wire bonding is being replaced by flip-chip, resulting in better impedance control of the signal path. To assess the high-frequency performance of a microvia to the embedded chip, a direct comparison to flip-chip interconnections is imperative. Necessary process steps as, for example, the redistribution layer, need to be taken into account. A direct measurement evaluation using dedicated test samples is very difficult, because for an adequate comparison the chip and board layout should be kept as identical as possible for both technologies. Manufacturing tolerances or sub-optimal design could outweigh the actual difference of the interconnection. For this reason, the comparison is limited to 3D full-wave simulations based on the finite element method (*Comsol Multiphysics*).

Deriving a general model for the microvia interconnect to an embedded chip is not as straight-forward, since the behaviour of the microvia strongly depends on its surroundings [48, 49, 50]. Boundary conditions, return current distribution and matching of the attached transmission lines need to be tightly controlled. This can be accomplished by either simulating only a small area around the interconnect or by de-embedding. The initial choice was to simulate a large geometry including launch structures to ensure a correct field distribution arriving at the discontinuity. Afterwards, the launch structures would be de-embedded using separate simulations of the individual structures. During set up, it became clear that the error on the de-embedding was sometimes larger than the parameters of the interconnect. As a backup option, the

geometry was reduced to the direct surroundings of the interconnect, with two short coplanar waveguides between the ports and the interconnect. The field distribution just before the interconnect is identical to the case with the longer launch structures and thus this backup option is used to compare the flip-chip solder ball interconnect with the microvia to the embedded chip.

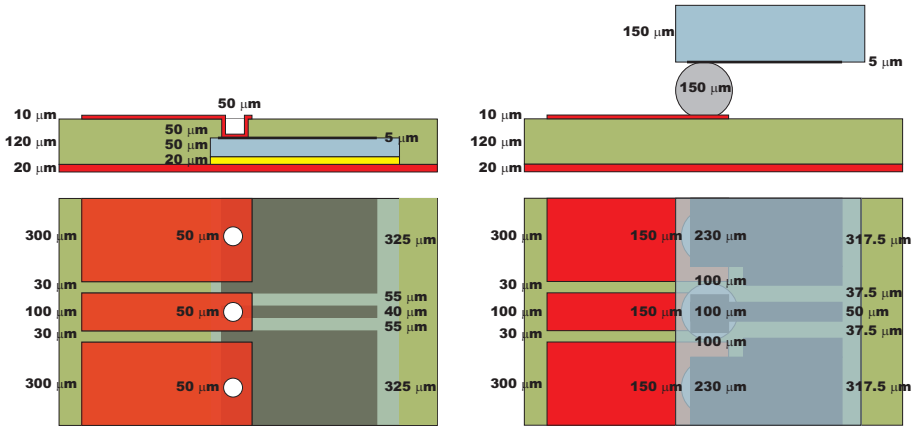


Figure 1.20: Simulation geometry for microvia to embedded chip (left) and the flip-chip solder ball interconnect (right). View from the top with partial transparency to reveal the structures below. The copper on the board is red, while the coplanar waveguide on the chip is represented in dark grey

The simulation geometry for both interconnect technologies is shown in Figure 1.20. Two ground connections are placed next to the signal pin to achieve a controlled return path. The width and spacing for the coplanar lines on the board, the embedded chip and the flipped chip are calculated to match the 50 Ω port impedance. The 200 µm long coplanar waveguide on the board is identical for both cases. The copper thickness on the board and inside the microvia is 10 µm, while the copper metallization on the chip is only 5 µm thick. The material for the solder ball is tin-silver-copper (SAC, $\sigma = 7.5\,\mathrm{MS/m}$). The pitch of the interconnection and the diameter of the ball or microvia are varied between simulations.

Figure 1.21 shows the S-parameters for the different combinations of pitch and ball or microvia diameter. The maximum insertion loss (S_{21}) is $-0.04\,\mathrm{dB}$ at 20 GHz and the corresponding reflection (S_{11}) is $-25\,\mathrm{dB}$. The latter is caused by the mismatch between the pitch of the interconnect and the spacing of the coplanar waveguide on the chip. Both interconnect technologies remain far below the typical insertion loss of a bond wire ($1 - 2\,\mathrm{dB}$ at 20 GHz [51]).

The return and insertion loss of the flip-chip interconnection show little influence from the pitch or ball size. For the microvia connection, there is a

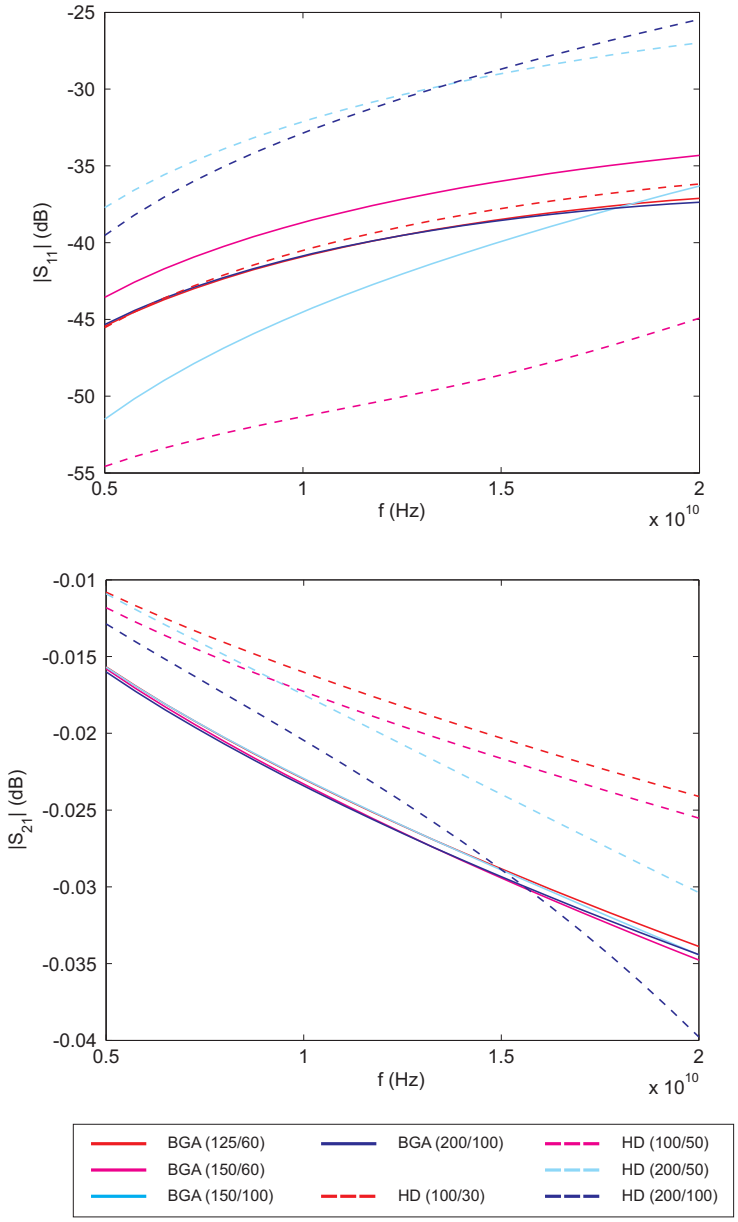


Figure 1.21: Simulation results for the interconnection to the chip. *BGA* refers to the flip-chip solder ball and *HD* denotes the microvia to embedded chip. Between brackets the connection pitch and the ball or microvia diameter are indicated in µm

clear link between the diameter of the via and the insertion loss. In general, the insertion loss of the microvia is slightly lower than the solder ball due to the difference in conductive material (copper versus SAC). Since the target land (on the chip) and capture land (on the board) of the microvia are varied with the hole diameter, a mismatch between the coplanar waveguides on the chip and the board is introduced when the land size differs from the width of the signal conductor. This is reflected in both the return and insertion loss. In conclusion, the shorter the interconnection, the better the high-frequency behaviour, provided there is a good match to the connecting transmission lines.

Note that only the interconnection to the chip itself is evaluated here. The flip-chipped die is typically placed on an intermediate substrate which is then mounted onto the printed circuit board. Chip embedding removes the need for an additional substrate, so the benefits of the microvia interconnection to the chip is even larger in this case.

1.3.3 Interference between the embedded chip and the board

Another major concern is the interference between signals on the embedded component and its surroundings. Due to the very low dielectric height above the chip, it is possible that critical signals on the board are disturbed by signals on the chip and vice versa. Metallization patterns on integrated circuits consist of multiple layers with dense routing. Because of the low dielectric separation between these layers, the coupling will primarily affect the adjacent traces on the chip itself. Embedded chips often require redistribution layers to adapt the pitch and placement of the bond pads to the requirements of the embedding process. These layers are typically less dense and thus more susceptible to crosstalk from the surroundings. The investigation here will be limited to the interference between traces on the redistribution layer and the board.

To verify the influence of the silicon on the crosstalk, the coupling factor between a trace on the redistribution layer and a trace on the board above the chip is determined. A quasi-static electromagnetic simulation (*Comsol Multiphysics*) is performed to determine the self and mutual capacitance and inductance of the traces. The geometry is shown in Figure 1.22. The redistribution layer consists of two layers of 5 µm thick polyimide. The distance between the traces, indicated by x_0, is varied from $-50\,\mu\text{m}$ to $100\,\mu\text{m}$. To mimic the presence of dense routing on the chip, additional simulations with a 1 µm thick ground plane between the silicon and the RDL are preformed. The backwards coupling factor is calculated as [52]

$$K_b = \frac{1}{4}\left(\frac{C_m}{C_l} + \frac{L_m}{L_l}\right). \tag{1.8}$$

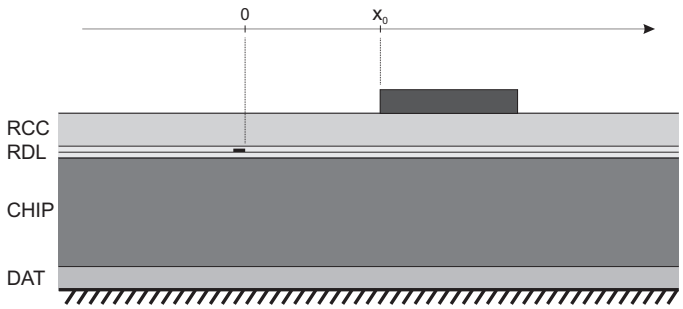


Figure 1.22: Simulation geometry for the crosstalk investigation between a trace on the redistribution layer and a trace on the board above the chip. ($w_{board} = 90\,\mu m$, $t_{board} = 17\,\mu m$, $w_{RDL} = 10\,\mu m$, $t_{RDL} = 1\,\mu m$, $h_{RCC} = 20\,\mu m$, $h_{RDL} = 2$ x $5\,\mu m$, $h_{CHIP} = 40\,\mu m$, $h_{DAT} = 20\,\mu m$, $\epsilon_{RCC} = 3.5$, $\tan\delta_{RCC} = 0.02$, $\epsilon_{PI} = 3$, $\epsilon_{Si} = 12.1$, $\sigma_{Si} = 10\,S/m$, $\epsilon_{DAT} = 3$)

Figure 1.23 presents the results of the simulations for the cases with and without ground plane. Especially at high frequencies, there is a strong coupling between the trace on the RDL and the trace on the board. In comparison, a $100\,\Omega$ differential microstrip pair has a coupling factor of about 0.15. The coupling factor consists of capacitive and inductive coupling. The latter is not affected by the conductivity of the silicon and slowly increases with frequency. The capacitive coupling shows a strong dependency on frequency. At low frequencies, the slow-wave propagation mode reduces the potential at the silicon surface. When the frequency increases, the displacement current in the substrate becomes dominant and the potential at the surface of the silicon starts to rise. As a result the mutual capacitance and thus the coupling factor increase with frequency. When the distance between the traces is large (green line in Figure 1.23), the potential difference along the surface of the silicon again reduces the coupling at high frequencies. For the case with the ground plane, the coupling factor decreases at frequencies below 1 GHz due to the finite thickness of the ground plane. The slow increase at higher frequencies is caused by the effect of the silicon on the potential of the floating ground plane. It is clear that the presence of the silicon increases the coupling between traces and is likely to affect the crosstalk between traces on the board above the chip in a similar way. The effect on the signal integrity of the entire system will depend on the specific components and on the actual routing on the chips and on the board.

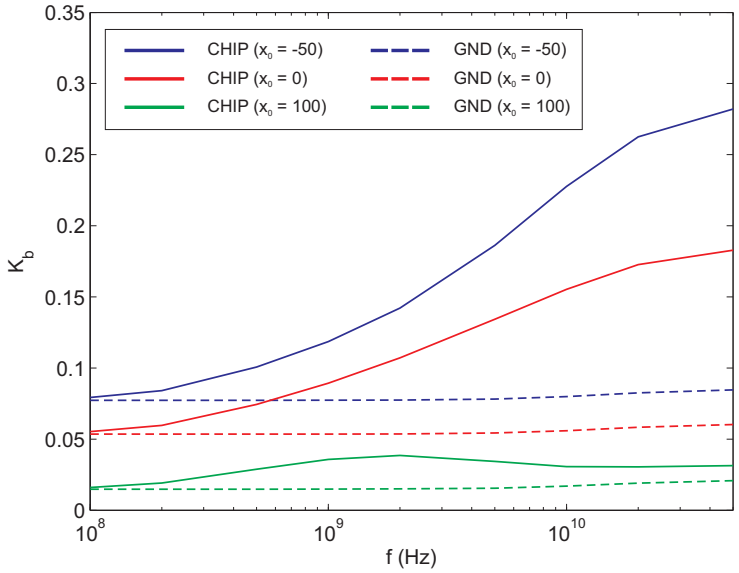


Figure 1.23: Simulation results for the interference between chip and board. *GND* refers to the situation with the additional ground plane

1.3.4 Advantage of embedded passive components

The optimal placement of passive components for decoupling or line termination can have a huge impact on the power and signal integrity. For embedded components, a number of new placement configurations become available. In addition, the possibility of embedding *passive* components results in even more design freedom. A detailed analysis is required to evaluate the drawbacks and benefits of each configuration.

Power distribution in complex printed circuit boards is implemented using power planes in combination with decoupling capacitors to reduce the power distribution impedance. The performance of the decoupling capacitors is degraded by the parasitic inductance (and resistance) in series with the capacitor. This inductance is a result of the effective series inductance (ESL) of the component itself in combination with the line inductance of the connection between the capacitor and the power planes. Embedding the decoupling capacitor in between the power planes minimizes the inductance of the interconnection and thus increases the resonance frequency of the power delivery network.

In appendix A, a detailed power integrity study is described that compares the behaviour of surface-mount devices and embedded components for power decoupling. It is found that when the layer count of the board is low, there is no significant difference between both technologies. When the number of

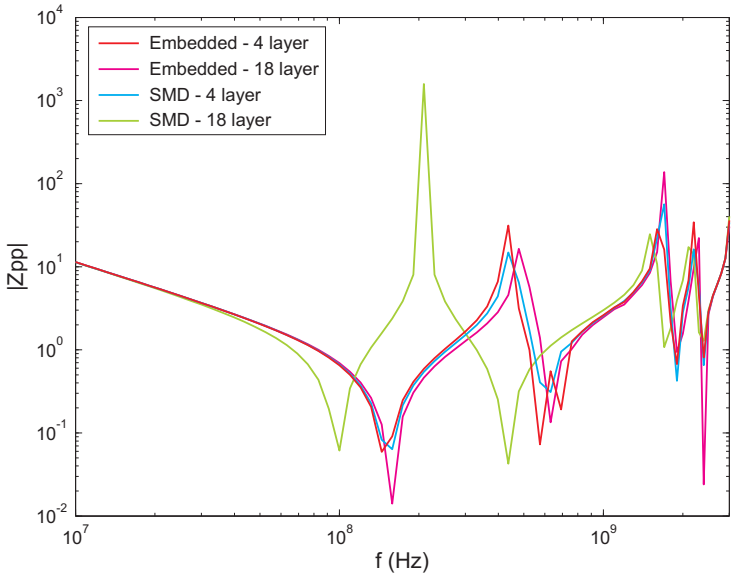


Figure 1.24: Comparison of embedded and surface-mount decoupling capacitors for a 4- and 18-layer board. (5 cm by 5 cm power plane pair with a 220 µm thick dielectric in between ($\epsilon_r = 3.9$). The excitation and measurement port are near the origin ($2\,\mathrm{x}\,10^{-3}$; $2\,\mathrm{x}\,10^{-3}$), while the decoupling capacitor is located at (0.04 ; 0.04))

layers increases, the short connection for the embedded components is clearly superior to the SMD capacitor. Figure 1.24 compares the simulation results for the 4-layer board to the 18-layer board, both with a 1 nF decoupling capacitor. The resonance for the embedded capacitor does not change significantly with the increased layer count. The case with the surface-mount capacitor however, shows a large increase in parasitic inductance due to the long vias through the board.

Chapter 2

Technology platform for the embedding of active components

Experience is a wonderful thing. It enables you to recognize a mistake when you make it again.

2.1 Introduction

Before the modelling of the high-frequency characteristics of embedded active components can start, a good understanding of the process steps used for this technology is required. The best way to do this, is to look at how the technology was developed. Since embedding active components in the build-up layers of a printed circuit board was not a mature technology at the start of this research, a significant amount of time was dedicated to establishing a reliable process flow. It is crucial to have a stable technology, otherwise the process variations will make a successful high-frequency characterization impossible.

In 2004, a European consortium was formed to transform the chip embedding principle into a production technology. The partners in the HIDING DIES project were *Nokia* (Finland), *Philips* (Netherlands), *AT&S* (Austria), *Datacon* (Austria), *CWM* (Germany), *TU Berlin* (Germany) and *IMEC*[1](Belgium).

[1]The Centre for Microsystems Technology (CMST) is a joined research group between the University of Ghent and the IMEC research institute. This doctoral research as a whole has been performed under the supervision and funding of the university; however, the official partner of the European project was IMEC.

The goal of the project was to develop a technology platform for embedding active components into printed circuit boards, suitable for production. In June 2007 the project ended, demonstrating the chip embedding technology on production scale equipment of the volume manufacturing line at AT&S. More advanced technology challenges such as ultra thin chips (down to 20 µm), large chip size (20 mm x 20 mm), fine pitch, and chip stacking were realized on a laboratory scale.

An overview of the technology platform for embedding active components in printed circuit boards is given in this chapter. The first section describes the specifications and the layout of the HIDING DIES test vehicles. Section 2.3 gives a short description of each of the process steps involved in the HIDING DIES technology, while going into more detail on the embedding process by vacuum lamination. The final section gives an overview of the reliability results and summarizes the technological achievements of the project.

2.2 Design of the HIDING DIES test vehicles

When developing a new technology, individual parts of the process flow can be tested initially using dummy substrates. To validate the entire process flow, there is a need for dedicated test vehicles, consisting of special test structures to verify the different aspects of the new technology: process parameters and variations, critical processing steps, yield assessment, reliability, ...

In order to investigate the technology platform for the embedding of active components and its reliability, a number of test vehicles were specified and designed within the HIDING DIES project. The test vehicles fall into three categories: A basic design used for the first assembly and evaluation (TV1), a thermal test vehicle (TV2), and an advanced technology test vehicle (TV3).

The first real design is TV1 and is meant for evaluating basic technology processes, yield and reliability. Specifications for TV1 are based on known PCB processing capabilities in order to reduce the risk of manufacturing the test vehicle and to concentrate on the embedding of dies. Since a significant part of the process flow is based on common printed circuit board processing steps, some of the selected test structures are derived from PCB process validation methods. Several variations of TV1 were designed, which in general consisted of:

- Different sizes of chips
  (2.5 mm x 2.5 mm, 5 mm x 5 mm, and 10 mm x 10 mm)
- Different pitch for the chips (200 µm and 300 µm)
- Thermal test chips for thermal management evaluation

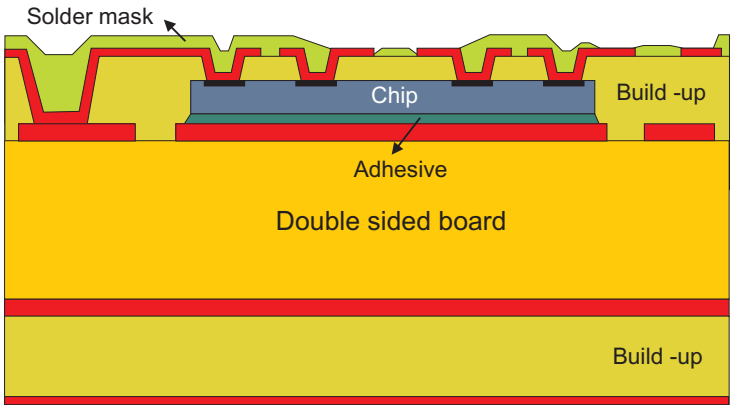


Figure 2.1: TV1.1 without PTH

- Daisy chains for testing the connections to the chips
- Four-point measurement test structures for resistance measurements
- Isolation test patterns
- High frequency test structures

Two different versions of TV1 were designed: one without plated through holes (PTH) (TV1.1 - Figure 2.1) and one with thermal through holes next to the die (TV1.2 - Figure 2.2). A third version with through holes underneath the die was planned, but later replaced by TV2. TV1.1 was intended for the first design and test runs, and for the development of the individual process steps, while TV1.2 was used for process optimization, yield assessment and reliability investigation.

The second test vehicle was designed to study the thermal management of embedded dies. TV2 uses the same thermal test chips as TV1, but has a simple layout, allowing easy measurements and thermal modelling. As in TV1, there are three implementations of the thermal test chips: one with cooling to the top, one with cooling to the back and the last with cooling in both directions. The layout and routing of these three implementations is kept as identical as possible to be able to correctly compare the measurement results and for easy modelling.

More advanced technology implementations, such as very fine pitch and stacking of embedded dies, were tested using a dedicated test vehicle. TV3 is a modular design, allowing not only different types of stacking, but the test vehicle also has the possibility to test certain aspects of the technology separately, without the need for fully populated boards or even the complete

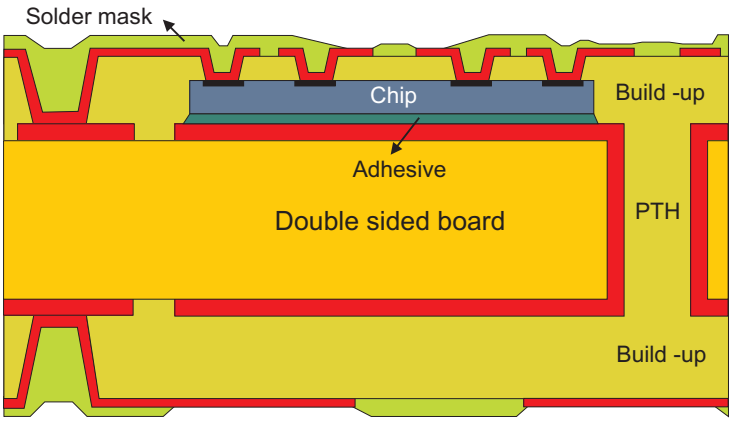


Figure 2.2: TV1.2 with PTH next to the die

build-up. The design consists of a six layer board with up to four layers of chips stacked on both sides of the board (Figure 2.3). Different stacking possibilities are implemented using small and large chips and by placing the upper chip out of the centre of the lower chip. Also the combination of passive components and flip-chip components with stacking of multiple dies can be investigated. Die bonding on structured copper areas gives an idea of the potential of the area underneath the chip for routing.

The complete specifications and details of the design for the *hiding dies* project are given in appendix B.

2.3 Process steps for embedding active components

The technology for embedding active components in printed circuit boards that is used for this research is built on the Chip in Polymer (CIP) concept, developed at the Technical University of Berlin. Within the HIDING DIES project, the technology process was further developed by using vacuum lamination for the embedding of the chips and printed circuit board technology for the generation of interconnections. One of the main benefits of this new technology is the use of established PCB and packaging technologies and production equipment (die bonding, vacuum lamination, microvia laser drilling) as well as the possibility for large area processing. The technology is compatible with microvia formation and integrated passive components used in advanced PCB manufacturing.

A schematic overview of the process flow for embedding chips is shown in

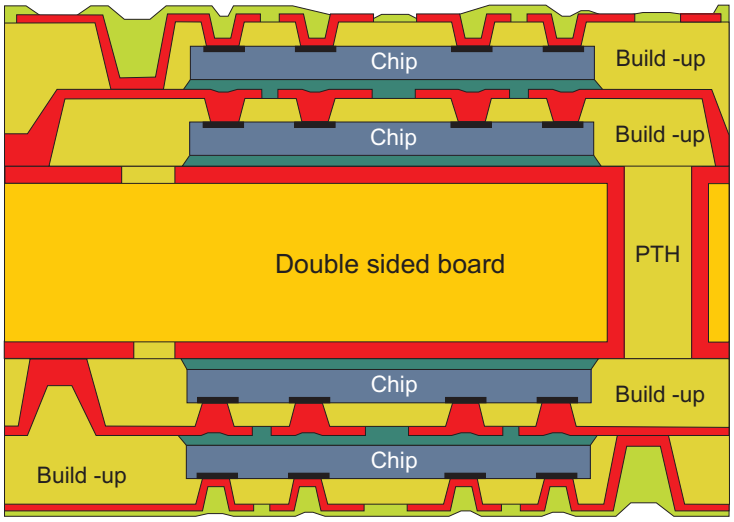


Figure 2.3: The advanced technology test vehicle (TV3)

figure 2.4. To be able to embed the chips into thin build-up layers, the chips need to be bumped and thinned down to 50 µm or below. The thinned chips are picked up from the wafer tape and placed on dedicated die bonding positions using local die bonding fiducials to maximize the placement accuracy. To take full advantage of the 3D packaging structure, the total thickness of the build-up layer should be kept as low as possible. The adhesive layer below the chip needs to be as thin as possible with excellent planarity. A non-planar adhesive layer may result in damage to the chip after lamination or create problems later on during microvia drilling and plating. The actual embedding of the chips into the PCB stack occurs in the vacuum lamination step. The core substrate with the die bonded chips is covered from both sides with a resin coated copper (RCC) layer. The lamination profile is a compromise between low pressure to protect the chips and high pressure for good flow and thermal contact. Due to the difference in thermo-mechanical behaviour of the different materials, there will always be a minimum amount of warpage and stress inside the board. Next to the warpage, the height of the RCC layer above the chip is one of the critical parameters. The thickness of the RCC layer is determined by the thickness of the die bond adhesive layer and the chip, the Cu bump height and the required height of the RCC above the chip. The height of the adhesive layer can be very well controlled and is usually about 20 µm. A $15 - 20$ µm epoxy layer on top of the embedded die offers a sufficient buffer for variations in chip and die bond adhesive thickness, while still maintaining the ability to create small microvias. The laser drilling of vias to the bond pads of embedded chips is

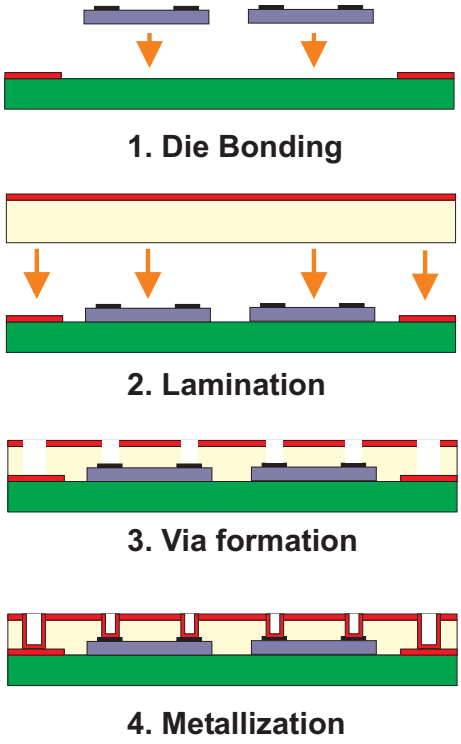


Figure 2.4: Process flow for embedding active components

comparable to the established formation of microvias on PCBs. In the first step the copper of the RCC above the pads of the chip is removed. Then the dielectric is removed by a laser until the Cu bump is reached. The final process step is the metallization, a combination of electroless and galvanic plating, and structuring of the copper by wet etching.

Below, a more detailed overview of the individual process steps is given. Most of these results were obtained by or in close corporation with other partners of the HIDING DIES project.

2.3.1 Wafer preparation

To interconnect embedded dies, it is necessary to prepare the bond pads of semiconductors with a PCB compatible surface finish. Standard chip metallization is aluminium, but this is not compatible with the copper metallization process. Bumping also makes it possible to enlarge the surface of the chip pad, assuming the I/O pitch is large enough. Several methods for bond pad

metallizations compatible with laser via drilling and via metallization are available. The best result for bond pad interconnection was reached with a copper metallization. Copper is fully compatible with the via metallization process.

First a 200 nm TiW and 300 nm Cu layer is sputtered on the full wafer. After sputtering, the copper seed layer is grown to a thickness of about 5 µm using electroless copper deposition. A photoresist layer is then applied and structured by a lithography process. The area of the bumps is covered. In the next step the Cu and TiW on the uncovered area are etched away and the photoresist is stripped. An alternative is to pattern plate the copper bumps by galvanic copper deposition. Both technologies require a lithography step, increasing the cost. Another compatible metallization is Ni/Pd. This is a low cost bumping technology and avoids complicated technologies like sputtering, etching and lithography. Electroless nickel is deposited only on the chemically activated aluminium chip pads. These bumps are covered with a thin palladium layer to ensure compatibility with the via metallization.

Chips with a very fine pitch ($< 100\,\mu m$) are, up to this point, not compatible with the combined alignment tolerances of the laser drilling and the copper structuring process (see also section 2.3.7). A possible workaround is the use of a redistribution layer to fan out the interconnections on the chip. To test the compatibility of the redistribution layer (RDL) with the chip embedding process, a number of test wafers with polyimide dielectric and 3 µm Cu from FCI (Flip Chip International), which is one of the leading service providers for bumping and wafer level CSPs, were evaluated. The RDL design is a daisy chain test pattern with 500 µm pitch and 300 µm pad size. There were no stress problem observed due to the polyimide layer in thinning, handling, embedding and interconnection processes.

For the embedding process using RCC, as in the HIDING DIES project, it is necessary to use dies thinned down to 50 µm. Wafer thinning of standard wafers by grinding and defect removal down is an established technology. The dicing-by-grinding (DBG) thinning process is less critical than conventional grinding. For the DBG process, the wafer is partially cut before thinning, with the cuts slightly deeper then the target thickness. After partial cutting, the active silicon surface is protected with grinding tape. During the backside grinding process there is no problem with warping of the wafer, because the surface of the wafer is divided into smaller areas by the incisions. As a result of the grinding process, the chips are separated on the grinding tape. The chips are then mounted on a UV release tape and ready for pick-up and die bonding. The biggest disadvantage of this technology is that it is not compatible with die attach adhesive film for die bonding, since this would require an additional step to cut the die attach tape.

A large selection of die bond adhesives is available in different physical formats, ranging from tape, over paste to liquid adhesives. Dicing die attach

tape offers the best planarity, thickness control and minimizes the risk of tool contamination. When thermal conductivity is required, an isotropic conductive adhesive paste offers the best compromise between processability and yield. This paste can be applied by screen printing and stencil printing, where the latter results in a smoother surface and constant thickness without voids.

Both conventional grinding in combination with a die attach tape (Lintec LE5000) as dicing-by-grinding combined with a printed adhesive (Heraeus PC 3001 silver filled paste) were evaluated during the project.

2.3.2 Die bonding

The thin wafers with singular chips are now moved to the die bonding equipment. The chips are ejected from the tape and moved to an intermediate bonding position. Here the actual position in X, Y and Θ of the chip is detected by pattern recognition on the bond pads or other clearly defined structures of the chip. The die bonding position on the board is determined either by global coordinates or by detecting local fiducials around the target area. The chip is picked up from the intermediate stage and moved to the final position. A combination of heat and pressing force secures the chip to the board, and the following baking step cures the adhesive.

The challenge of thin chip die bonding is to achieve a low adhesive thickness. The embedding into a build-up layer limits the allowed thickness of chip and die bond adhesive. The combined height of chip and adhesive should be less than the available dielectric thickness, leaving about $15 - 20\,\mu m$ of dielectric over the chip after embedding. Otherwise a planar embedding is impossible and the chip might get damaged.

A large number of tapes and eject systems are available and the right combination needs to be selected for every single application. The parameters of the UV curing, especially exposure time and UV intensity also have a big influence on the ejecting process. For the chip release from the dicing tape, non-penetrating needle ejectors are well known to be suitable for a chip thickness down to $50\,\mu m$ and chip sizes up to $100\,mm^2$. To increase the process window in terms of lower chip thickness, larger die size and higher eject speed and to decrease mechanical stress in the ejected component, a new needle-less eject principle was developed by Datacon. The eject device consists of a 3D shaped surface without any moving parts. Needle-less eject systems based on different production technologies were designed, manufactured and tested during the project.

2.3.3 Chip embedding

A classic lamination cycle is composed of a temperature profile and a pressure profile. These parameters are determined by both material characteristics and design requirements. The temperature profile normally starts with a controlled temperature ramp-up using a well defined heating rate, up to a maximum temperature which is maintained for a certain amount of time. The heating rate and the length and height of the temperature plateau are determined by the material characteristics, but are limited by external factors such as the thickness of the press book, machine parameters, and cost. By choosing a certain heating rate, it is possible to control the viscosity of the RCC during lamination, and thus how much the resin flows. Too much flow can cause some areas to be depleted, while insufficient flow will create voids. The amount of flow is also determined by the pressure that is applied during lamination. The pressure must be high enough to equally distribute the resin across the board and to assure sufficient adhesion to the layer below. The pressure at the start of the cycle, the so-called kiss pressure, has to be high enough to give a good thermal contact, but without damaging the chips. When the temperature rises, the RCC first starts to melt. For a certain heating rate and at a specific temperature the viscosity of the resin will reach a minimum. After that, when the temperature continues to rise, the resin will start to cure. In order to fully cure the RCC, the board must stay above the curing temperature for a sufficient amount of time. The RCC used for the chip embedding during the HIDING DIES project is the Hitachi MCF6000E and the fluidity curves are shown in Figure 2.5. The curing requirements are 40 minutes above 175 °C.

The first lamination trials were performed using the standard AT&S lamination cycle for the Hitachi material on dummy boards and on the very first TV1 design (TV1.1A). The lamination results were very good from the beginning, however some optimizations were needed. Printed circuit board manufacturers use a separate cooling press to cool down the boards after lamination, to avoid the additional time needed to heat-up the main lamination press. There is no need for a separate cooling press in the laboratory, so an extra cooling phase under pressure was added at the end of the cycle to reduce the warpage of the boards. The goal for further optimizations was to reduce the length of the cycle, to be able to laminate more boards per day, and at the same time maintain or even improve the quality of the lamination. After the first trials with the AT&S cycle, a strong print-through of the chips and the copper structures on layer S2 arose. To reduce this effect, the IMEC cycle starts with a lower kiss pressure and a 15 min evacuation period before the temperature ramp-up. The maximum temperature has been reduced, since the temperature drop over the thin press book used in the laboratory is very small (Figure 2.6).

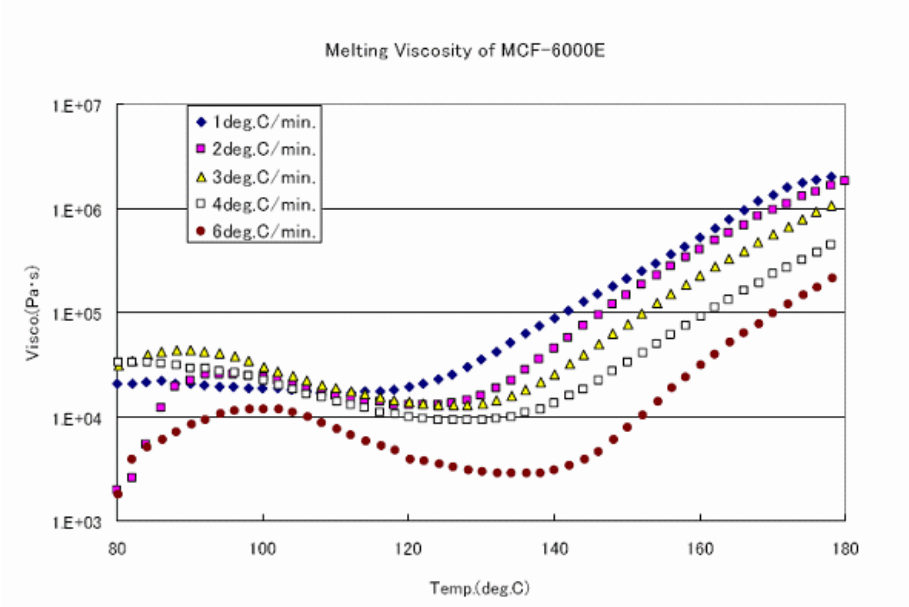


Figure 2.5: Fluidity curves for Hitachi MCF 6000E

2.3.4 Via formation

Laser drilling has been the preferred method for microvia generation for several years. Initially, a conformal mask laser drilling method was used, where the copper openings are created by a photolithography process and wet etching followed by a laser drilling step, where the top copper layer acts as a mask for the CO_2 laser. Nowadays, high-speed systems using UV lasers, hybrid UV - CO_2 combinations or CO_2 direct drilling offer increased flexibility, lower cost and higher throughput. For small substrates and on a laboratory scale however, the increased control of wet etching in combination with CO_2 drilling outweighs the speed advantage of UV laser drilling.

The biggest disadvantage of the wet etching to open the vias at our site is the use of glass masks. The alignment of these masks can only be done using global fiducials, one set for the entire board, and can not be adjusted to deformations of the board during processing. Another problem was that it was very difficult to find a good fiducial design which was easy to open up using the laser and still allowed for a very precise alignment. The yellow light from the aligner strongly reduces the contrast between the copper of the fiducials and the dielectric underneath it. This was even worse for TV3, since the fiducials for the second layer were placed on a background of transparent RCC. As a

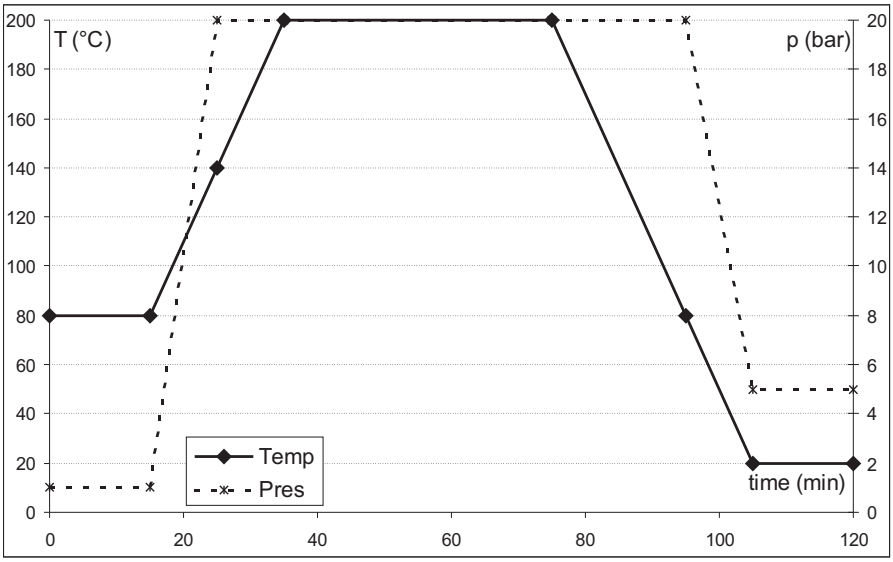


Figure 2.6: Optimized IMEC_HD_2 lamination cycle with lower kiss pressure (1 bar) and reduced maximum temperature (200 °C)

result, there were some slight misalignments during processing. Due to the large pads used on TV1, this was not really an issue; however for the fine pitch on TV3 this was very critical (Figure 2.7). Industrial via formation systems using laser drilling are more flexible regarding alignment (see section 2.3.7).

A second issue with via formation is the dependency on the thickness of the RCC above the chips. When using a Nd:YAG laser (3rd harmonic: 355 nm) to open the copper, the laser beam penetrates into the RCC by punching through the copper. If the amount of RCC above the chip is too low, the YAG laser could damage the copper bumps on the chips. For the CO_2 drilling, the thickness itself does not really matter, since it will stop on the copper pads anyway; however to optimize the parameters for drilling, this height must be as constant as possible. During processing it became clear that there was a large variation in chip thickness, causing a similar variation in RCC thickness above the chip. When chips from different grinding runs are embedded into the same board, this could become an issue for the CO_2 drilling parameters. Production level grinding equipment should have tighter tolerances to overcome this difficulty. Another cause for variation in RCC thickness above the chips is the difference in die bond layer thickness between chips bonded on structured copper versus copper planes. Since part of the die bond adhesive flows in between the copper tracks underneath the chips, the height of the die bond

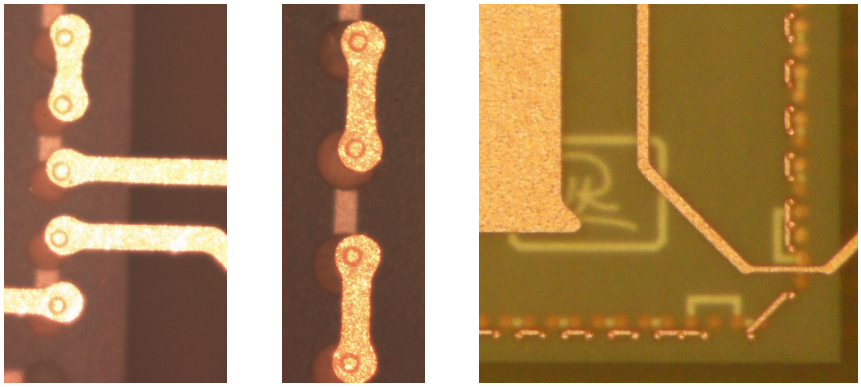


Figure 2.7: Microvia alignment on TV1 and TV3. Left: Via hits the pad of the 200 µm pitch chip on TV1; Middle: Via hits the pad of the 300 µm pitch chip on TV1; Right: Misalignment is too big to hit the pad of the 100 µm pitch on TV3

layer plus the chip is reduced, resulting in more RCC above the chip. This will be something to take into account at the design stage.

2.3.5 Metallization

The metallization process consists of Palladium activation, followed by electroless copper and finally galvanic copper deposition. The process parameters do not differ much from those used for standard printed circuit board plating.

After laser drilling, the boards go through a desmear cycle to clean out the hole and to prepare it for the electroless copper plating. The first step is an alkaline bath containing glycol ether solvents to swell the epoxy resin, followed by another alkaline bath containing $KMnO_4$, which attacks the epoxy resin for surface roughening. Cleaning the substrate is done by using an acidic bath containing hydrogen peroxide to neutralise the agents from the previous bath. Finally the epoxy surfaces are conditioned for subsequent catalyst adsorption. The electroless copper starts with a micro etch, to roughen the copper surface in order to achieve micro-anchoring of the electroless Cu. This step is limited in time not to remove too much copper from the bumps on the chips. To prevent harmful drag-in from the previous oxidizing baths to the catalyst bath, a predip is required. The catalyst is a colloidal bath containing stannous chloride and palladium chloride and deposits the palladium catalysts on well treated epoxy surfaces by adsorption. Stannous hydroxide is formed when rinsing after activation. The following accelerator step solubilizes these hydroxides, activating the palladium. Now the boards are ready to enter the electroless copper

bath, where $1 - 2\,\mu m$ of copper is deposited.

In order to deposit sufficient copper inside the microvias to the chips without plating too much on the top copper, a low current density was used for the galvanic plating. A thickness of $10\,\mu m$ to $15\,\mu m$ of copper on the walls of the via seems to be enough for a reliable contact. This results in a total copper thickness of $15\,\mu m$ to $20\,\mu m$ on the top, which is already the maximum to allow for the fine lines and spacing on TV3.

Copper structuring at our site is done by photolithography and spray etching (cupric chloride etchant). When the pitch of the chip pad is decreasing, issues concerning alignment become more and more apparent. Laser direct imaging (LDI) avoids the need of an etch mask by directly illuminating the photoresist with a laser beam, offering increased alignment flexibility. Small pitches also impose new restrictions on the line width and the spacing for tracks connecting these chips. For example, a $100\,\mu m$ pitch chip requires a line width and track spacing of $50\,\mu m$, which is even at the limit for advanced PCB production technologies. Traditional copper structuring uses a subtractive process: the copper is plated to the required thickness and afterwards the copper is removed in the areas between the lines. The high copper thickness causes more under etching, making it difficult to produce fine lines. Pattern plating, which is the industry standard nowadays, only deposits copper in the areas where the tracks are going to be, while the other areas are protected by a plating resist. This process relies on thick base copper and uses plated solder as etching resist for the traces. The metal plating resist requires an alkali etchant that has an inferior etching factor. The semi-additive process overcomes these difficulties by using an ultra thin plating base, which can be removed by an etching process without the need for a metal resist to protect the electroplated copper. This reduces the risk of under etching and allows for very fine lines and spacing down to $25\,\mu m$.

2.3.6 Chip stacking

Embedding of active components into the build-up layers of a printed circuit board was successfully investigated during the processing of the first test vehicle. Optical inspection and reliability tests showed that the lamination quality was very high. The next challenge is to stack multiple dies on top of each other and to investigate the influence of asymmetrical build-ups, double sided bonding and different combinations of chips. All these aspects are incorporated in the advanced technology test vehicle TV3. This section will give an overview of the lamination results of TV3 and the chip stacking efforts on a laboratory scale.

The advanced technology test vehicle

TV3 was designed to investigate advanced technology implementations such as fine pitch, chip stacking and die bonding on structured copper. The focus of this section will be on the last two. Figure 2.3 shows the build-up of TV3: a double sided core, with two build-up layers containing embedded dies on each side. Two sizes of chips are used, resulting in four different stacking combinations on each side of the board. Thanks to the modular design of TV3, several different implementations, such as asymmetrical build-ups and eccentrically placed chips, can be investigated. An overview of the different stacking combinations is shown in Figure B.12 of appendix B.

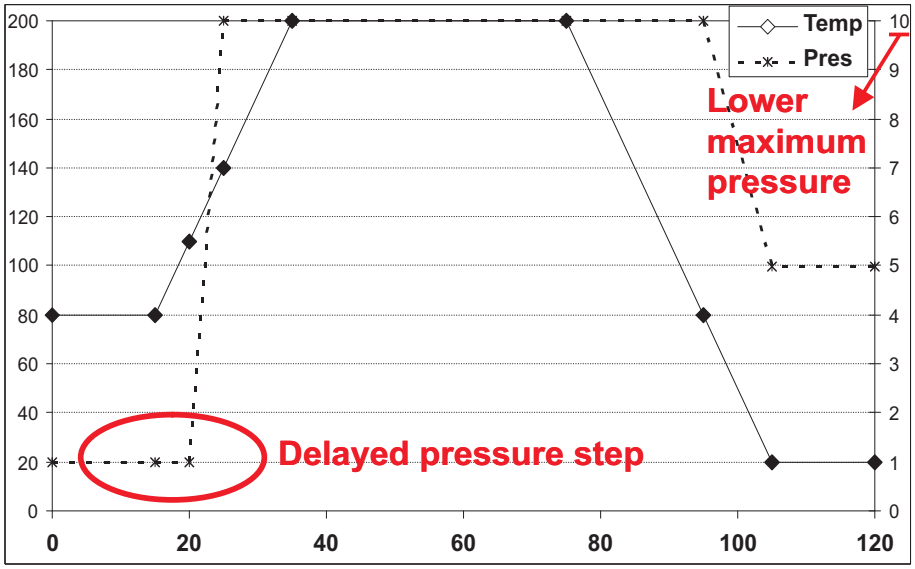
Lamination profile

To successfully stack embedded components, the stress created in the components needs to be minimized. On the other hand, a good resin flow, or high pressure, is required to have an equal distribution of RCC over the chips. A compromise between these two requirements is needed. Detailed investigations performed by TUB showed that one of the critical parameters is the moment at which the full pressure is applied. Based on actual temperature measurements inside the stack-up during lamination, the optimal point for the application of the pressure ramp is determined. This resulted in a delayed pressure application (after 20 min in stead of 15 min). To reduce the risk of chip cracking as a result of an uneven die bonding surface or warpage of the layer below, the maximum pressure was lowered from 20 bar to 10 bar. The temperature profile from the standard lamination cycle used for TV1 remained the same. The adjusted profile is shown in Figure 2.8(a). A new and prolonged lamination profile featuring a lower heating rate (3 degrees per minute versus 6) for better control of the viscosity was also tested (Figure 2.8(b)). This profile is based on the one used at TUB.

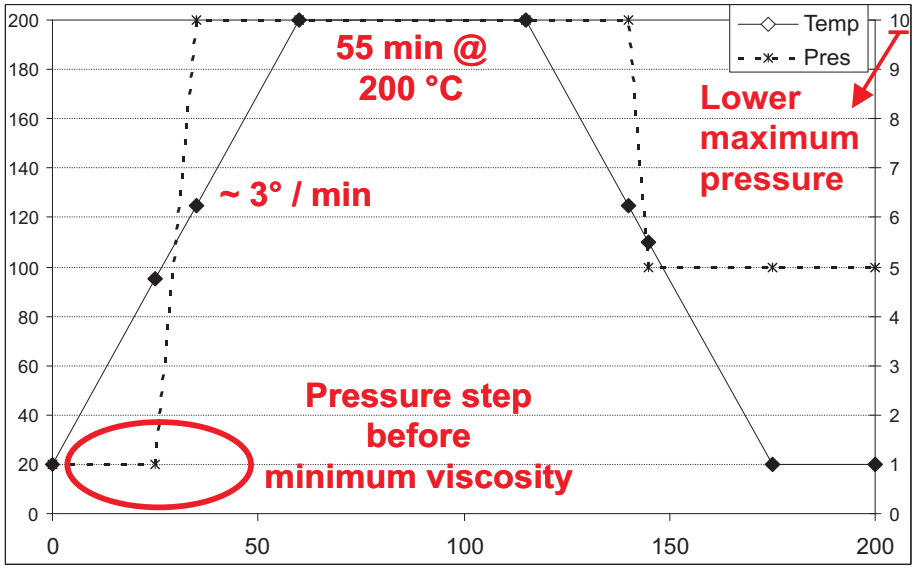
Apart from the lamination profile, the actual stack up used during lamination was also optimized. An extra sheet of release foil and a small Teflon sheet were added to create a buffer for pressure changes and for a better spreading of the pressure over the substrate. Both stack-ups can be compared in Figure 2.9. The direct influence of these adaptations is less clear and probably more difficult to implement in a production environment where multiple stack-ups are laminated at a time.

Lamination results

The first run of TV3 boards was started with 4 samples: TV3_D2 to TV3_D5. After the processing of the first layer, cross-sections were made from the TV3_D3 board. The three remaining boards were each laminated with a differ-



(a) IMEC_HD_TV3



(b) IMEC_HD_TV3_2

Figure 2.8: Lamination profiles for chip stacking

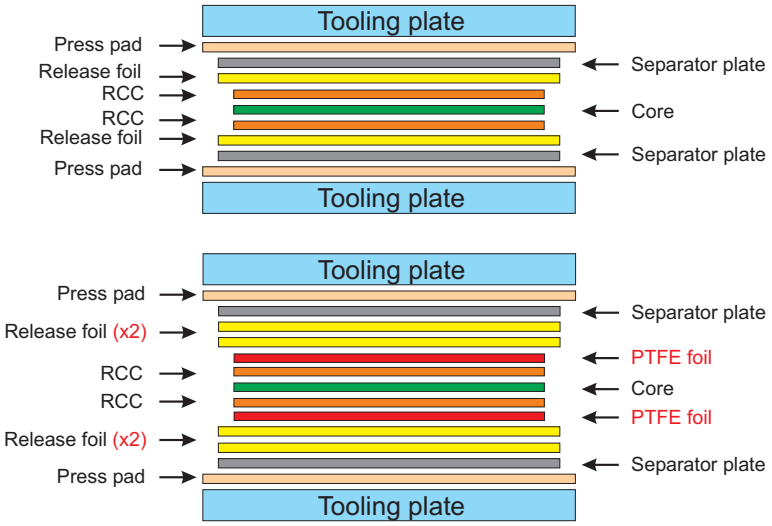


Figure 2.9: Comparison of the lamination stack-up for single-chip embedding (top) and for chip stacking (bottom)

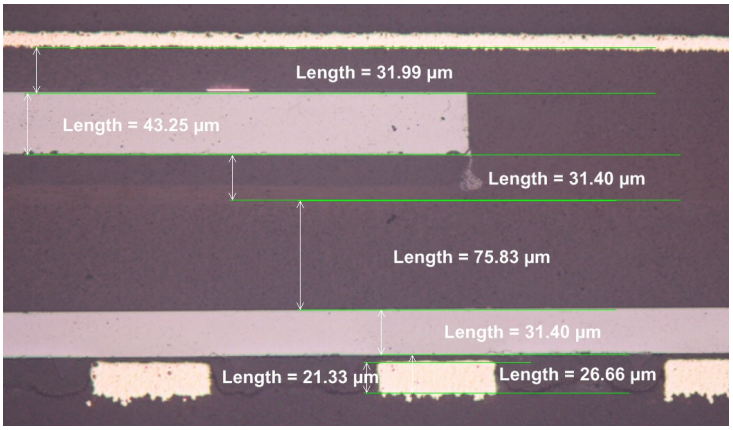


Figure 2.10: A small chip on top of a larger chip. Notice the 75 µm of RCC above the chip as a result of the very thin chip and the die bonding on structured copper

ent profile: TV3_D2 with the adjusted IMEC_HD_TV3 profile, TV3_D4 with the prolonged IMEC_HD_TV3_2 profile and finally TV3_D5 with the standard IMEC_HD_2 profile (Figure 2.6), which was also used for the first layer of chips. Cross-sections were made of all the boards after lamination to compare the lamination results.

Overall, the lamination of the second layer of chips was quite successful. Some cracks were detected at the points where the upper chip is overlapping the lower, but in general the results were very good. Notice also the large amount of RCC above the chips in the first layer (Figure 2.10). The reason for this is the very thin chip used here (30 µm thickness in stead of the expected 50 µm) in combination with the low amount of die bond tape above the structured copper.

From the measured heights and the visual inspection of the cross-sections, it is clear that the lamination pressure is a very important parameter. The standard lamination cycle, as used for TV1, reveals several smaller and larger cracks for chips placed on die bond locations with uneven surfaces, either from structured copper or due to the chip below. This is emphasized when looking at the small chips that were placed eccentrically on top of a larger chip. Due to the presence of the large chip, there is some difference in height of the first build-up layer underneath the small chip. An extra difficulty was created during the design, since there is no copper underneath the part of the small chip that is not overlapping the chip below, increasing the thickness difference between both ends of the chip. In Figure 2.11, a reconstruction is made from module 5 on the TV3_D4 board. Comparing the thickness of the die bond layer at the

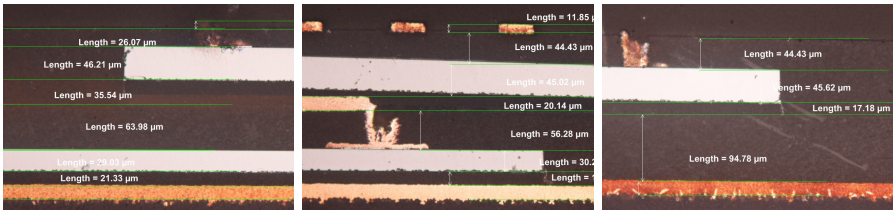


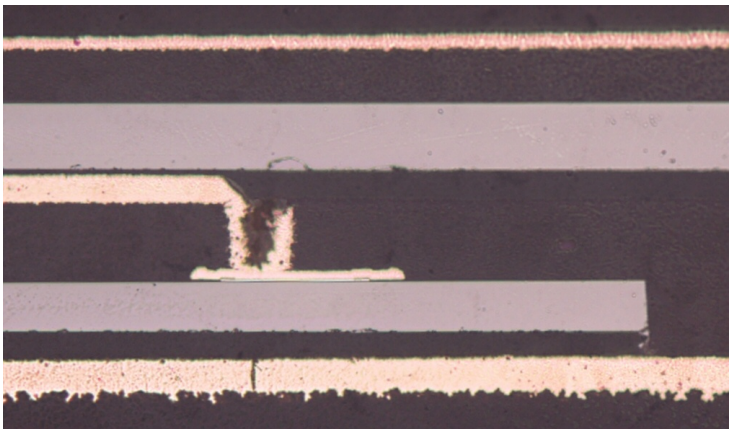
Figure 2.11: A 5 mm by 5 mm chip stacked eccentrically on top of a 10 mm by 10 mm chip, with copper routing underneath the lower chip. The overhanging chip is slightly tilted, but no cracks occurred. Notice also the difference in thickness between the two chips

edge above the large chip (35.54 µm) to the other end of the chip (17.18 µm), it is clear that the chip is slightly bended. Although it is barely visible on the picture, the adhesive tape in the left hand cross-section came loose from the board and resin has flown between the tape and the surface of the first build-up layer.

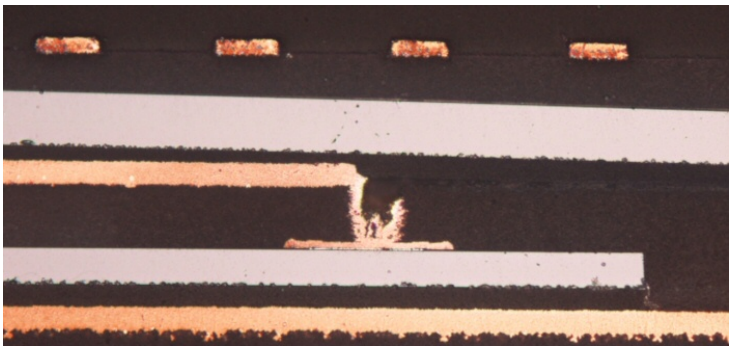
Figure 2.12 shows a close-up from this same location for the different lamination profiles. The two profiles using a lower pressure show similar bending of the chip without cracks. The chip from the TV3_D5 board, laminated with 20 bar maximum pressure, is cracked above the end of the copper track. While lowering the maximum pressure seems to be a good solution to prevent the chip from cracking, the chip is still bended resulting in a difference in height of the RCC above the chip. This can create difficulties for the laser drilling and plating of the microvias to the chips. Another solution could be not to cure the die bond adhesive before lamination, allowing the adhesive to flow and thus levelling the chip. It can also be made into a design rule that an even distribution of the copper underneath the chip is required. These last two recommendations could then allow the use of a higher pressure, insuring a better resin flow and distribution across the board.

Not only the lamination parameters, but also the die bonding circumstances are important for a crack-free stacking of embedded chips. The choice for curing the adhesive tape before or during lamination can be critical. The advantages of curing directly after die bonding are good adhesion and the fixation of the chip to prevent movement after placement. If the die bonding surface is flat, for example in the case of a copper plane, this is the best option. When bonding on structured copper, there is a risk that either the tape curls up between the copper tracks or voids are created underneath the chip.

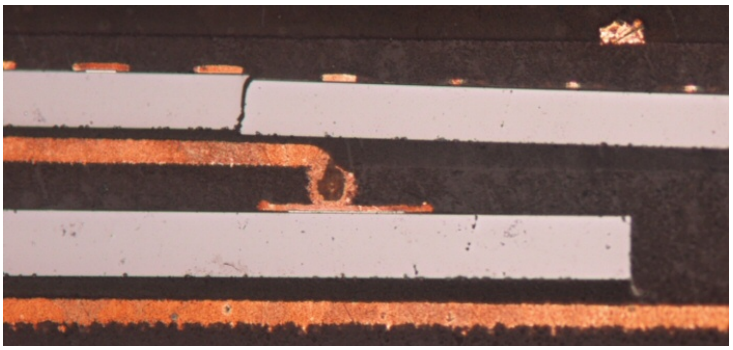
The main focus of the advanced technology evaluation was on chip stacking rather than on fine-pitch chips. No major issues were discovered during lamination, thanks to the precautions taken and adjustments made to the lam-



(a) TV3_D2



(b) TV3_D4



(c) TV3_D5

Figure 2.12: Close-up from a small chip overlapping a large chip

ination process. A number of different stacking combinations were tested: a symmetrical build-up with chips on both sides of the board, an asymmetrical build-up with only chips on the upper two build-up layers, and only one layer of chips in the second build-up layer. For these combinations, no repeatable failures occurred during lamination.

The most critical parameters for chip stacking are the maximum pressure, the flatness of the die bonding surface and the curing of the die bond adhesive. A compromise between these three parameters makes it possible to adapt the chip stacking technique for different applications. This can be done either at the design stage by making the die bonding locations as flat as possible or during processing by optimizing the die bonding and lamination parameters.

2.3.7 Alignment accuracy

To make chip embedding a competitive packaging technology, the minimum pitch and pad size need to be comparable to other packaging solutions. For example, state-of-the-art flip-chip interconnects achieve pitches below 150 µm. Extremely fine pitches offered by wire bonding (< 40 µm) are however beyond the reach of the current technology. The minimum pitch realised with the proposed embedding technology is 100 µm on a laboratory scale, while pitches down to 60 µm are expected to be feasible.

The minimum pitch is determined by the pad size on the chip that is necessary to achieve a reliable interconnection. The required pad size depends on the microvia drill diameter and the alignment accuracy. For instance, a drill diameter of 50 µm combined with an alignment accuracy of ± 25 µm leads to a minimum pad size of 100 µm and thus a pitch of 150 µm. The smallest microvia drill diameter is limited by the laser drilling process, in this case the spot size of the YAG laser, and the plating process, which requires a minimal aspect ratio of $1:1$, meaning the height of the via equals the diameter. A drill diameter as low as 30 µm has been realised in the lab. To achieve a pitch below 100 µm using this diameter, the overall accuracy needs to be better than ± 20 µm.

The inherent accuracy of the chip embedding process is determined by the die bonding, the laser drilling and the copper structuring. An important aspect for obtaining the highest accuracy is fiducial design. Using local fiducials around the die bonding position, a very high placement accuracy can be achieved (10 µm @ 3σ). Laser drilling can use global fiducials for the whole board or panel, or local markings for areas requiring higher accuracy. Multiple layers and chip stacking increase the number of fiducials, with additional restrictions to their placement. The fiducials for the build-up layers need to be slightly shifted with respect to each other. The reason for this is that the copper and the resin of the layer above the fiducial are removed to be able to visualize the fiducial. So this area can not be used to place the fiducials for the

next layer. All these alignment marks require some free space around them, imposing limitations on the routing. For the copper structuring, one mask is used for the complete board, so local adjustments cannot be made. The accuracy is further hindered by board deformations caused by thermal expansion of the core during the lamination process. On a 10 cm by 10 cm sample, a plastic deformation of about 60 µm in one direction was measured and thus the position of the chip pad is altered by the same amount. Since this deformation is not uniform in all directions, advanced scaling algorithms are needed to match both the laser drilling design and copper layout to the distorted board. Flexible imaging systems such as laser direct imaging (LDI) are crucial for achieving these high densities on a large printed circuit board substrate.

2.3.8 Reliability results

Table 2.1: Overview of reliability tests

Test	Test details
Humidity storage	85 °C/85% RH, 1000 h
Humidity storage under bias	85 °C/85% RH, 10 mA, 1000 h
Thermal storage	150 °C, 1000 h
Thermal cycling	−40 to 125 °C, 1000 cycles
Reflow	3 x Pb-free profile

Reliability tests were originally intended to be performed on the first test vehicle to investigate the performance of the chip embedding platform at the industrial partners (Datacon, AT&S). Due to delays in the processing caused by various reasons, the initial testing was performed on samples that were manufactured by the research institutes. Based on these early results, a test strategy was developed to investigate the reliability of the samples supplied by AT&S. Table 2.1 gives an overview of the reliability test performed within the project. Note that the humidity storage under bias was performed using a DC current to stress the via interconnection, but this does not correspond to a standard bias test. Each sample was electrically tested by measuring the DC resistance of one of the 21 daisy chains present in the TV1 design. The chains are divided into sub chains, so a defect can be located more precisely and broken parts can be shorted, taking them out of the measurement chain. Apart from electrical testing, all parts were inspected optically for possible mechanical defects and cross sectioned if further inspection was needed.

Overall a significant number of contacts to the chip were investigated, although only a limited amount of samples were available for testing (Table 2.2). Delamination occurred for two samples after humidity storage and reflow

Table 2.2: Overview of reliability results

Test	Contacts	Electrical defects	Delamination
Humidity storage	3002	6	1 sample
Humidity storage (bias)	1704	0	No
Thermal storage	1232	0	No
Thermal cycling	4712	8	No
Reflow	1018	0	1 sample

testing. In both cases a separation between chips and the silver-filled epoxy adhesive layer occurred. It should be noted that the interconnection to the chip did not fail electrically. The majority of the defects occurred for boards that initially already showed a large number of failed daisy chains. Cross sectioning revealed that this was due to a faulty metallization process, resulting in large voids inside the plated vias. Based on the results for these samples we could state that the chip embedding process shows promise for good reliability.

2.4 Conclusion

Within the HIDING DIES project, a technology platform which allows for the embedding of thin dies into the build-up layers of high-density PCBs was successfully developed. Chip embedding was demonstrated on production scale equipment at AT&S's volume manufacturing line. However chip embedding is still not mature for volume manufacturing. Next to the additional technology development, questions like supply chain, end-to-end design environment and testing have to be addressed. However, the focus here lies on the technical challenges, requiring future research efforts.

A summary of the technological achievements is given in Table 2.3. The accomplishments are split up in those that were realised on production equipment and successful trials on a laboratory scale. Technological progress on a production scale will mainly come from new and improved manufacturing equipment and better integration of the supply chain. The substrate size for example is still limited by the capabilities of die bond equipment. During the project manufacturing was done up to half-size panels (18" x 12"). A continuous production on a large standard panel, like 18" x 24", is still not implemented. There was no clear influence discovered from the chip technology (CMOS, analog), but breaking due to a brittle multilayer metal/passivation stack did occur. This is a problem that could be taken into consideration upstream.

At IMEC and TUB, laboratory scale and semi-automatic equipment was used for the process development work. Developments were mainly done with

Table 2.3: Technology achievements of the HIDING DIES project

Parameter	Technology platform	Feasibility study
Technology level	production	laboratory
Substrate size	18" x 12"	10 x 10 cm^2
Chip thickness	50 µm	30 µm
Chip size	$\leq$ 10 x 10 mm^2	20 x 20 mm^2
Chip I/O pitch	200 µm	100 µm
Via technology	with lands	landless
Interconnects	50 µm L&S	50 µm L&S
Stacked chip levels	1	2

panel formats of 10 x 10 cm^2, while the thinnest chips that were embedded had a thickness of 30 µm. At Datacon pick-up and bonding of chips down to 20 µm thickness was developed, as well as picking and bonding of chips up to 20 x 20 mm^2 and 50 µm thickness. In the feasibility phase no additional effort was spent to achieve high density lines and space geometries, however developments in this area are crucial for the embedding of ultra fine pitch chips. Due to a lack of remaining resources, work was done on 2 layers of embedded chips. The evaluations did not show principle barriers for additional layers.

In the TV2 modules, a thermal test chip was embedded and evaluated by Philips. Testing was done up to 1 W dissipation. The measured data was in good accordance with the thermal model. The model shows that the bottle neck for heat flow is the core substrate. In order to achieve much higher power dissipation a high density of thermal vias is required. Here the development of other solutions like embedding of heat sinks might be necessary.

The goal for the industrialisation of embedding technologies is a new integrated manufacturing line to offer low cost solutions for high density electronic systems. The new manufacturing process should combine PCB processing and die assembly in one production line to avoid difficulties of transport between different manufacturing plants. Far-reaching changing to the existing PCB manufacturing flow and infrastructure are required: More advanced conveyor systems, software modifications for automated optical inspection, electrical testing methodologies, standardization of software tools and design formats, and a thorough yield analysis to reduce expensive scrap of production panels with embedded components.

Chapter 3

Modelling and Simulation

Real life is grey, but the golden tree of theory springs ever green.
vrij naar Johann Wolfgang von Goethe

This chapter gives an overview of the different approaches to modelling tracks running on top of embedded components. The first section gives a detailed description of the classical approach using the parallel-plate waveguide as a wide strip limit for the microstrip.

A theoretical approach to determine the high-frequency behaviour of a waveguide is based on the calculation of the propagation constant by performing a mode analysis of the cross-section of the waveguide. This can be done analytically for simple waveguides such as the parallel-plate waveguide or the rectangular waveguide. More complex waveguides require advanced numerical techniques to determine the propagation modes and often 3D electromagnetic simulators are used to obtain a solution. Section 3.2 takes a closer look at some of these techniques applied to the multilayer microstrip geometry.

3.1 The parallel-plate approximation

3.1.1 Literature

The high-frequency problem of tracks running on top of embedded dies shows quite some resemblance to the problem of microstrip interconnects on integrated circuits [53, 54, 55]. An exact mode analysis of the wave propagation along a microstrip on a $Si - SiO_2$ system requires solving an extremely difficult eigenvalue problem. For this reason the microstrip is often treated as a perturbation of the parallel-plate waveguide, which is a reasonable approximation if the width of the strip is much larger than the height of the substrate. Already in

1967, Guckel et al. [53] introduced the concept of different propagating modes depending on the working frequency and the conductivity of the silicon. They were also the first to perform a simple mode analysis on a parallel-plate loaded with a dielectric layer and a conductive layer. Based on the propagation constant, a circuit model was introduced, first as a low frequency approximation where the conductive layer acts as a metal, later adding second order effects such as loss in the semiconducting layers and the effect of high conductivities. The authors also give some meaningful expressions about the high frequency behaviour.

One of the base references concerning microstrip interconnects on integrated circuits was published by Hasegawa et al. in 1971 [54]. In this paper, a theoretical and qualitative analysis of the propagation modes and the corresponding electromagnetic field distribution is given. By introducing the concept of the effective permittivity and permeability, not only the behaviour of the different propagation modes can be described, but also the transitional regions between these modes. Hasegawa et al. start from the parallel-plate waveguide, showing that the behaviour of this structure can be divided into three regions, depending on frequency and silicon conductivity. For high frequencies and low silicon conductivity the waveguide can be regarded as a sandwich of two dielectric layers. The fundamental propagation mode closely resembles a quasi-TEM mode. When the silicon conductivity is high, the depth of penetration at high frequencies will become equal to or smaller than the silicon thickness. The wave propagates almost entirely through the lossless dielectric, with the silicon acting as an imperfect ground plane. The third region is referred to as the slow-wave mode. Due to strong interfacial polarization between the conducting and non-conducting media, the effective dielectric constant increases to values far above those of the two materials. This interfacial polarization was first described by Maxwell and Wagner, and a detailed discussion can be found in [56]. This polarization effect occurs when two touching dielectrics differ in conductivity and therefore require different voltage gradients to carry a current of constant density. Typical for this slow-wave mode is the very low propagation velocity and a minimal attenuation constant for a given conductivity.

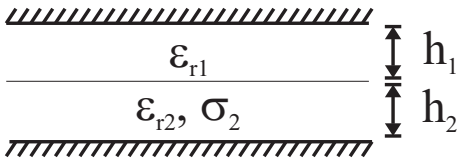


Figure 3.1: The parallel-plate approximation as used by Hasegawa et al.

A mode analysis of the parallel-plate waveguide in figure 3.1 reveals a TM wave as fundamental propagation mode. The complex longitudinal and transverse propagation constants of this mode are linked together by the material

parameters

$$\gamma_i^2 + \gamma^2 = -\omega^2 \epsilon_i^\star \mu_i^\star \qquad i = 1, 2 \tag{3.1}$$

where γ_i is the transverse propagation constant in the dielectric ($i = 1$) or conductive layer ($i = 2$), and γ the longitudinal propagation constant. $\epsilon_i^\star = \epsilon_i' - j\epsilon_i''$ and $\mu_i^\star = \mu_i' - j\mu_i''$ represent the complex permittivity and permeability of each layer [1]. In order to determine the propagation constant γ, additional boundary conditions are added: perfect magnetic conductors to limit the width of the geometry and continuity at the inner boundaries. Instead of solving the Helmholtz wave equation for the magnetic field directly, using the boundary conditions to calculate the field distributions and the propagation constant γ, the transverse resonant method [57] was used to obtain the propagation constant.

$$\sum_{i=1}^{2} \frac{\gamma_i}{j\omega\epsilon_i^\star} \tanh \gamma_i h_i = 0 \tag{3.2}$$

where h_i is the thickness of each layer.

A quantitative description of the transmission properties of the parallel-plate waveguide is performed by Hasegawa et al. [54] by introducing the complex effective permittivity and permeability, which are defined based on the material parameters and waveguide geometry, in such a way that the propagation constant can be expressed as

$$\gamma = j\omega\sqrt{\epsilon_{eff}^\star \mu_{eff}^\star} \tag{3.3}$$

The fundamental mode of the parallel-plate waveguide exhibits three different propagation modes, depending on the frequency f and the conductivity of the conductive layer σ_2. The real parts of the effective permittivity and permeability can now be used to describe each of these three modes.

1. Dielectric quasi-TEM mode

$$\epsilon_{eff}' = \epsilon_0 \epsilon_{r\infty} \qquad \mu_{eff}' = \mu_0 \tag{3.4}$$

where $\epsilon_{r\infty}$ is the optical value of the Maxwell-Wagner permittivity.

$$\epsilon_{r\infty} = \frac{h_1 + h_2}{\dfrac{h_1}{\epsilon_{r1}} + \dfrac{h_2}{\epsilon_{r2}}} \tag{3.5}$$

This can be considered as the geometrical average of the dielectric constant of the two layers.

[1] The $\star$ symbol is used to explicitly denote the complex nature of the material parameter. This is not to be confused with the $*$ symbol, referring to the complex conjugate

2. Skin effect mode

$$\epsilon'_{eff} = \epsilon_0 \epsilon_{rs} \qquad \mu'_{eff} = \mu_0 \frac{1}{h}\left(h_1 + \frac{\delta}{2}\right) \tag{3.6}$$

where ϵ_{rs} is the static value of the Maxwell-Wagner permittivity, δ the depth of penetration into the conductive layer and h the total height of the waveguide.

$$\epsilon_{rs} = \epsilon_{r1} \frac{h}{h_1} \tag{3.7}$$

$$\delta = \sqrt{\frac{2}{\sigma_2 \omega \mu_0}} \tag{3.8}$$

$$h = h_1 + h_2 \tag{3.9}$$

3. Slow-wave mode

$$\epsilon'_{eff} = \epsilon_0 \epsilon_{rs} \qquad \mu'_{eff} = \mu_0 \tag{3.10}$$

Note that the static value is only determined by the dielectric constant of the non-conductive dielectric layer and the thickness ratio of the two layers. In the case of a very thin dielectric layer, it can reach very high values, larger than those of the individual layers.

A visual way to represent the different regions of propagation depending on frequency and conductivity is the resistivity-frequency domain chart. From the mode analysis of the parallel-plate waveguide, the frequencies defining the transitions between the different regions for a given silicon conductivity can be determined [54]. The transition from the slow-wave mode to the dielectric region is characterized by the dielectric relaxation frequency of the silicon layer f_e and the relaxation frequency of the interfacial polarization f_s.

$$f_e = \frac{1}{2\pi} \frac{\sigma_2}{\epsilon_0 \epsilon_{r2}} \tag{3.11}$$

$$f_s = \frac{1}{2\pi} \frac{\sigma_2}{\epsilon_0 \epsilon_{r1}} \frac{h_1}{h_2} \tag{3.12}$$

The transition frequency for the skin effect region can be calculated by comparing the depth of penetration to the thickness of the silicon layer.

$$f_\delta = \frac{1}{2\pi} \frac{2}{\mu_0 \sigma_2 h_2^2} \tag{3.13}$$

The thickness of the silicon used for embedding components in the build-up layers of printed circuit boards is around 50 µm, with smaller thickness expected in the future. Even for high conductivity silicon (σ_2 =10^3 S/m), the

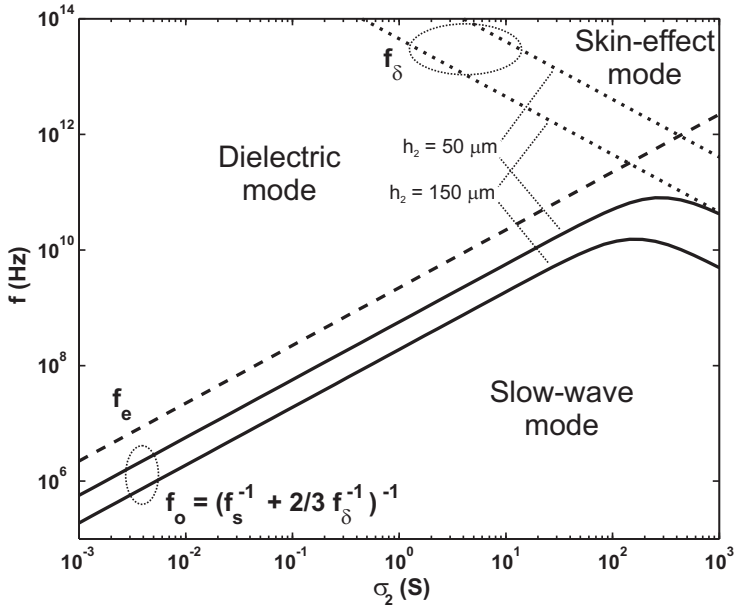


Figure 3.2: Resistivity-frequency domain chart for the thickness found in embedded active components ($h_1 = 20\,\mu\text{m}$, $h_2 = 50\,\mu\text{m}$). Even for a silicon thickness of 150 µm, the onset of the skin effect mode is above 10 GHz

transition frequency f_δ for thin chips is above 100 GHz, so beyond the targeted frequency range (100 MHz to 20 GHz). The resistivity-frequency domain chart for thickness commonly found for embedded active components is shown in figure 3.2.

The three propagation modes are linked together by transitional regions which can be described by the relaxation behaviour of the effective permittivity for the transition from the slow-wave mode to the dielectric mode and the relaxation of the effective permeability for the transition from the slow-wave mode to the skin effect mode. The effective dielectric constant is subject to a Debye-type relaxation with the relaxation time constant determined by f_e and f_s.

$$\epsilon'_{reff} = \epsilon_{r\infty} + \frac{\epsilon_{rs} - \epsilon_{r\infty}}{1 + \omega^2\tau^2} \tag{3.14}$$

$$\epsilon''_{reff} = (\epsilon_{rs} - \epsilon_{r\infty}) \frac{\omega\tau}{1 + \omega^2\tau^2} \tag{3.15}$$

where

$$\tau = \tau_e + \tau_s = \epsilon_0 \frac{h_2}{\sigma_2} \left(\frac{\epsilon_{r1}}{h_1} + \frac{\epsilon_{r2}}{h_2} \right) \tag{3.16}$$

The frequency dependent behaviour of the real and imaginary part of the effective dielectric constant is determined by the conductivity of the conductive layer (σ_2) and by the static (3.7) and optical value (3.5) of the Maxwell-Wagner permittivity.

The transition from the slow-wave region to the skin effect mode can be approximated by the following expressions [54].

$$\frac{\mu^{\star}_{eff}}{\mu_0} = 1 - \frac{h_2}{h} F(f/f_\delta) \tag{3.17}$$

where

(3.18)

$$F(f/f_\delta) = 1 - \frac{1}{\gamma_m h_2} \tanh \gamma_m h_2 \tag{3.19}$$

and

(3.20)

$$\gamma_m h_2 = (1+j)\sqrt{f/f_\delta} \tag{3.21}$$

A better understanding of where expressions (3.4) to (3.16) come from can be gained by going back to the description of the interfacial polarization by von Hippel [56]. The classical example of interfacial polarization is the Maxwell-Wagner two-layer condenser (figure 3.3), which is basically a parallel-plate capacitor filled with two conductive dielectrics ($\epsilon_1, \sigma_1, h_1$ and $\epsilon_2, \sigma_2, h_2$). Figure 3.3 also shows the equivalent circuit, where each layer is represented by a shunt connection of a resistor and a capacitor.

$$C_1 = \frac{A}{h_1}\epsilon_1 \qquad C_2 = \frac{A}{h_2}\epsilon_2 \tag{3.22}$$

$$R_1 = \frac{h_1}{A\sigma_1} \qquad R_2 = \frac{h_2}{A\sigma_2} \tag{3.23}$$

Here, A is the surface of the plate capacitor. The admittance of this equivalent circuit is

$$Y = \frac{1 + s\left(R_1C_1 + R_2C_2\right) + s^2 R_1R_2C_1C_2}{R_1 + R_2 + s\left(R_1R_2\left(C_1 + C_2\right)\right)} \tag{3.24}$$

At low frequencies ($s \to 0$), this admittance becomes a series connection of the two resistors. When the frequency is high ($s \to \infty$), the circuit behaves as a series combination of the two capacitors. Using the expressions for the resistance and the capacitance, the relaxation time constant of the admittance can be written as

$$\tau = \frac{R_1R_2\left(C_1 + C_2\right)}{R_1 + R_2} = \frac{\epsilon_1 h_2 + \epsilon_2 h_1}{\sigma_1 h_2 + \sigma_2 h_1} \tag{3.25}$$

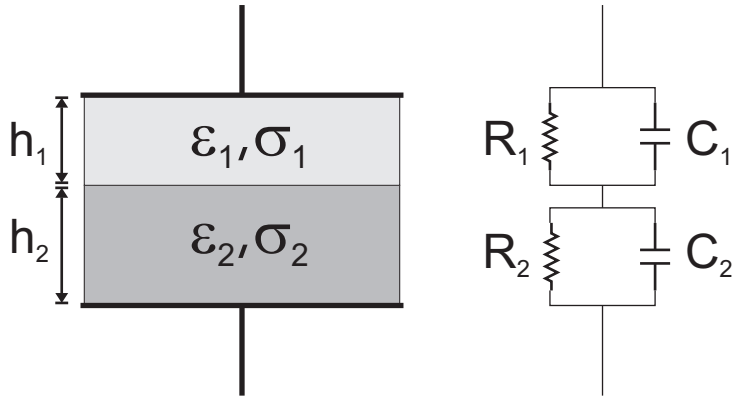


Figure 3.3: Maxwell-Wagner two-layer condenser filled with two conductive dielectrics and the corresponding equivalent circuit

The admittance can be related to the classic expression for a parallel-plate capacitor to determine the effective dielectric constant.

$$\epsilon'_{reff} = \epsilon_{r\infty} + \frac{\epsilon_{rs} - \epsilon_{r\infty}}{1 + \omega^2\tau^2} \tag{3.26}$$

$$\epsilon''_{reff} = \frac{\sigma}{\omega} + (\epsilon_{rs} - \epsilon_{r\infty}) \frac{\omega\tau}{1 + \omega^2\tau^2} \tag{3.27}$$

where

$$\epsilon_{rs} = \frac{R_1C_1 + R_2C_2 - \tau}{R_1 + R_2} \tag{3.28}$$

$$\epsilon_{r\infty} = \frac{R_1C_1R_2C_2}{R_1R_2\left(C_1 + C_2\right)} \tag{3.29}$$

The ohmic conductivity term in (3.27) is caused by the series resistor $R_1 + R_2$.

A similar calculation can be performed when the conductivity of the first layer is set to zero ($\sigma_1 = 0$). This is equivalent to removing the resistor R_1 from the circuit in figure 3.3. The admittance becomes

$$Y = \frac{sC_1\left(1 + sR_2C_2\right)}{1 + sR_2\left(C_1 + C_2\right)} \tag{3.30}$$

with the relaxation time constant

$$\tau = R_2\left(C_1 + C_2\right) = \frac{h_2}{\sigma_2}\left(\frac{\epsilon_1}{h_1} + \frac{\epsilon_2}{h_2}\right) \tag{3.31}$$

The expression for the effective dielectric constant remains the same, apart from the ohmic conductivity term that disappears, but the values for ϵ_{rs} and

$\epsilon_{r\infty}$ can now be calculated explicitly. When the conductive current in the second layer is much higher than the dielectric current, the capacitor C_2 can be regarded as an open and thus the equivalent capacitance is only determined by C_1. This leads to the expression of ϵ_{rs}. When the dielectric current is higher, the resistor R_2 can be ignored and the expression of $\epsilon_{r\infty}$ appears.

$$C_{eff} = \frac{\epsilon_s A}{h_1 + h_2} = \frac{\epsilon_1 A}{h_1} \qquad \Leftrightarrow \qquad \epsilon_{rs} = \epsilon_{r1} \frac{h_1 + h_2}{h_1} \tag{3.32}$$

$$C_{eff} = \frac{\epsilon_\infty A}{h_1 + h_2} = \frac{A}{\frac{h_1}{\epsilon_1} + \frac{h_2}{\epsilon_2}} \qquad \Leftrightarrow \qquad \epsilon_{r\infty} = \frac{h_1 + h_2}{\frac{h_1}{\epsilon_{r1}} + \frac{h_2}{\epsilon_{r2}}} \tag{3.33}$$

These equations are exactly the same as the ones derived from the mode analysis by Hasegawa et al [54].

Williams investigates the one-dimensional Metal-Insulator-Semiconductor transmission line as an alternative to the parallel-plate waveguide [58]. The transmission line consists of a metal film limited on one side by a magnetic wall and separated by an insulator from a semiconductor substrate backed with a perfectly conducting wall (figure 3.4). The magnetic wall approximates the nearly open-circuit condition at the air-metal interface on top of the signal line, while the electric wall simulates the boundary condition due to the highly conductive metal film on the back of the substrate. The mode analysis of the waveguide reveals a TM wave, who's propagation constant and field distribution can be solved exactly by defining the complex permittivity of the different layers.

A simple model, composed of the circuit elements found in [53, 54, 55] and for this reason called the "conventional model" by Williams, is based on the surface-impedance (R, L) and parallel-plate-capacitor (G, C) approximations. This model gives a good estimate for the conductance and capacitance per-unit-length in the low-loss and slow-wave region, and for the resistance and inductance per-unit-length in the slow-wave and the skin effect regions. However, the conventional model breaks down for thicker semiconductor layers. A better model can be derived using the exact integral expressions for the per-unit-length parameters [59]. While these expressions are valid for any transmission line, they require the closed-form approximations of the field distribution in the waveguide. These can be solved analytically by only evaluating the modal voltage v_0, the modal current i_0 and the integrals in the semiconducting substrate, which is a good approximation for very thin metal and insulating

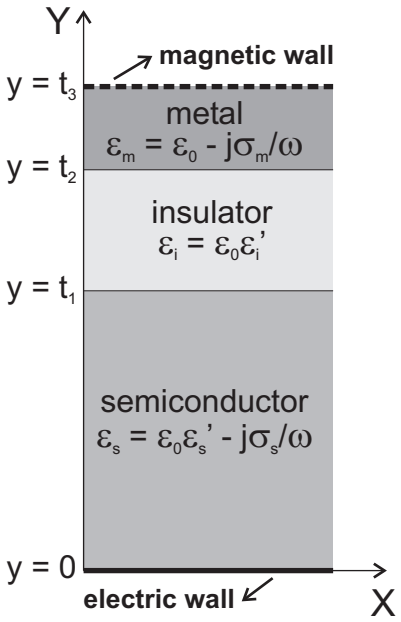


Figure 3.4: Metal-Insulator-Semiconductor transmission line

layers.

$$R + j\omega L = \frac{j\omega}{|i_0|^2} \int_{y=0}^{h} \left(\mu_0 \left| H_x \right|^2 - \epsilon^\star \left| E_z \right|^2 \right) \mathrm{d}y \tag{3.34}$$

$$G + j\omega C = \frac{j\omega}{|v_0|^2} \int_{y=0}^{h} \epsilon^\star |E_y|^2 \mathrm{d}y \tag{3.35}$$

where h is the total height of the waveguide. Although the integral model offers the possibility of very accurate closed-form expression valid over the entire range of operating conditions, the model still fails to describe the behaviour of microstrips with a width smaller than the height of the waveguide. A direct comparison by Williams reveals that the fringing fields cannot be ignored, especially in the case of the resistance and the inductance per-unit-length [58]. In order to accurately describe the propagation behaviour of a microstrip on a dielectric and semiconductor substrate, more advanced models are required. These will be introduced in section 3.2.

Application to embedded chips

As stated above, the parallel-plate model was developed to analytically describe interconnects on integrated circuits. The geometry for embedded active com-

ponents in printed circuit boards is however quite different from the situation on integrated circuits (figure 3.5). The insulating layer of the metal-insulator-semiconductor transmission line, usually consisting of SiO_2, is very thin (about 1 µm) compared to the silicon thickness (up to 600 µm). This is however not the case for embedded active components, due to the use of thinned chips (about 50 µm thickness) and laminated RCC as dielectric (in the order of 20 µm above the chip). Between the chip and the underlying copper layer, there is a die bonding adhesive, which can be a polymer die attach tape (DAT) but also a conductive paste. Typical printed circuit board characteristics as high track thickness, surface finish and solder mask have to be regarded in the final analysis.

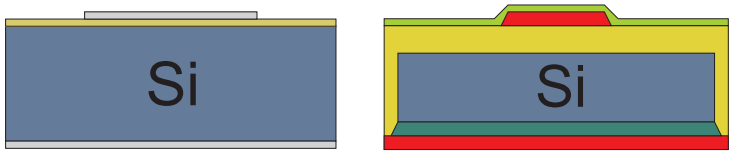


Figure 3.5: Comparison of the geometry of interconnects on integrated circuits (left) versus printed circuit boards (right)

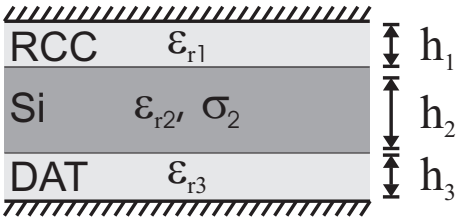


Figure 3.6: Geometry for the parallel-plate approximation loaded with three layers

The first major difference that needs to be studied is the influence of the third material layer, since there are now two interfaces at which the Maxwell-Wagner polarization occurs (figure 3.6). The formula for the optical value of the Maxwell-Wagner permittivity $\epsilon_{r\infty}$ is based on the calculation of the effective dielectric constant of a two-layer dielectric mixture and can easily be expanded to three layers.

$$\epsilon_{r\infty} = \frac{h_1 + h_2 + h_3}{\frac{h_1}{\epsilon_{r1}} + \frac{h_2}{\epsilon_{r2}} + \frac{h_3}{\epsilon_{r3}}} \tag{3.36}$$

For the two-layer structure, the static value of the Maxwell-Wagner permittivity is calculated from the interfacial polarization between the dielectric and the silicon. If the dielectric is assumed to be non-conductive ($\sigma_1 = 0\,\mathrm{S/m}$), only

the dielectric constant of the RCC is included in the formula for ϵ_{rs}. Adding the die bonding adhesive layer, which is also assumed to be non-conductive, the new value of ϵ_{rs} becomes an averaging of the dielectric constant of the RCC (ϵ_{r1}) and of the die attach tape (ϵ_{r3}).

$$\epsilon_{rs} = \frac{\epsilon_{r1}\epsilon_{r3}}{\frac{h_1}{h}\epsilon_{r3} + \frac{h_3}{h}\epsilon_{r1}} \tag{3.37}$$

where h is the total height of the substrate.

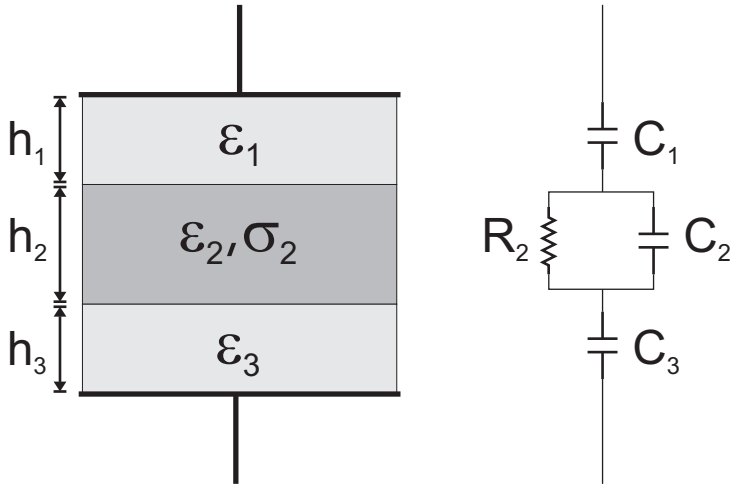


Figure 3.7: Maxwell-Wagner condenser filled with one conductive layer and two dielectric layers and the corresponding equivalent circuit

The values for the static and the optical value of the effective dielectric constant above, as well as the transition from the slow-wave mode to the dielectric region can be derived by adding an extra layer to the Maxwell-Wagner condenser (figure 3.7). The admittance of this new structure becomes

$$Y = \frac{sC_1C_3\left(1 + sR_2C_2\right)}{C_1 + C_3 + sR_2\left(C_1C_2 + C_2C_3 + C_3C_1\right)} \tag{3.38}$$

This leads to the following expression for the relaxation time constant.

$$\tau = R_2\frac{C_1C_2 + C_2C_3 + C_3C_1}{C_1 + C_3} = \frac{h_2}{\sigma_2}\frac{\frac{\epsilon_1}{h_1}\frac{\epsilon_2}{h_2} + \frac{\epsilon_2}{h_2}\frac{\epsilon_3}{h_3} + \frac{\epsilon_3}{h_3}\frac{\epsilon_1}{h_1}}{\frac{\epsilon_1}{h_1} + \frac{\epsilon_3}{h_3}} \tag{3.39}$$

The complex effective dielectric constant is again obtained by calculating the

equivalent capacitance.

$$\epsilon'_{reff} = \epsilon_{r\infty} + \frac{\epsilon_{rs} - \epsilon_{r\infty}}{1 + \omega^2\tau^2} \tag{3.40}$$

$$\epsilon''_{reff} = (\epsilon_{rs} - \epsilon_{r\infty}) \frac{\omega\tau}{1 + \omega^2\tau^2} \tag{3.41}$$

with

$$C_{eff} = \frac{\epsilon_s A}{h_1 + h_2 + h_3} = \frac{A}{\frac{h_1}{\epsilon_1} + \frac{h_3}{\epsilon_3}} \quad \Leftrightarrow \quad \epsilon_{rs} = \frac{h_1 + h_2 + h_3}{\frac{h_1}{\epsilon_{r1}} + \frac{h_3}{\epsilon_{r3}}} \tag{3.42}$$

$$C_{eff} = \frac{\epsilon_\infty A}{h_1 + h_2 + h_3} = \frac{A}{\frac{h_1}{\epsilon_1} + \frac{h_2}{\epsilon_2} + \frac{h_3}{\epsilon_3}} \quad \Leftrightarrow \quad \epsilon_{r\infty} = \frac{h_1 + h_2 + h_3}{\frac{h_1}{\epsilon_{r1}} + \frac{h_2}{\epsilon_{r2}} + \frac{h_3}{\epsilon_{r1}}} \tag{3.43}$$

3.1.2 Simulations

In the previous section, an overview was given of the various models based on the parallel-plate waveguide. Due to the specific differences in geometry between interconnects on integrated circuits and microstrips running on top of embedded components, certain adaptation to these models were required. The most important modification is the addition of a third layer. To verify the validity of these modifications, a 3D finite element method (FEM) electromagnetic simulator was used to calculate the field distributions for the propagation modes.

The simulations were performed using the RF module of Comsol Multiphysics. To obtain a basic understanding of the phenomena occurring due to the combination of conducting and non-conducting layers, a quasi-electrostatic simulation of a parallel-plate capacitor was performed. A fixed voltage is placed on the top plate and the frequency is swept for a given conductivity of layer 2. If the conductivity σ_2 is much larger than $\omega\epsilon_0\epsilon_{r2}$, there will be no potential difference across the semiconductor. The total potential is divided between the two dielectric layers, inversely proportional to their dielectric constant. When the frequency rises, $\omega\epsilon_0\epsilon_{r2}$ becomes larger than σ_2 and the potential difference across the semiconductor increases. At the high-frequency limit, providing the skin effect region is not reached, the potential is spread across the three layers, again inversely proportional to the dielectric constant of each layer.

A broadband, full wave mode analysis was also performed by regarding the parallel-plate as a waveguide structure, revealing the propagation constant for a given frequency. The propagation constant γ can then be used to calculate the real and imaginary part of the effective dielectric constant.

$$\gamma = \alpha + j\beta \tag{3.44}$$

$$\alpha = \frac{1}{2}\left(\frac{2\pi f}{c}\sqrt{\epsilon'_{reff}}\frac{\epsilon''_{reff}}{\epsilon'_{reff}}\right) \tag{3.45}$$

$$\beta = \frac{2\pi f}{c}\sqrt{\epsilon'_{reff}} \tag{3.46}$$

The first geometry consists of a simple parallel plate with the following materials: a 20 µm dielectric layer (RCC: $\epsilon_{r1} = 3.8$), a 50 µm thick silicon layer ($\epsilon_{r2} = 12.1$) and a 20 µm dielectric layer (DAT: $\epsilon_{r3} = 3$). These numbers are based on the practical dimensions and material parameters as found in the embedding of active components in printed circuit boards. Since these simulations where only performed to verify the parallel-plate approximation, no extended parameter sweep was performed. The width of the parallel-plate capacitor was 2 mm. Figure 3.8 shows the comparison of the simulation results with formula (3.40) for the real part of the effective dielectric constant. The behaviour of the simulated parallel-plate capacitor fits exactly with the formula. Varying the conductivity of the silicon shifts the curves according to the change in the relaxation frequency f_e, but the step-like shape remains the same. The results from the mode analysis, for σ going form 0.1 S/m to 10 S/m, also correspond well with the formula, although the relaxation frequency of the simulation is slightly higher than predicted by the analytical model. At low frequencies (below 50 MHz), the effective wavelength becomes too large for the mode analysis to give reliable results. Figure 3.9 shows the results for the attenuation constant which is independent of frequency above f_e and increases quadratic with frequency for frequencies below f_e. Again, the formula for the imaginary part accurately predicts the simulation results. Due to the very low values of the attenuation constant at low frequencies, the erratic behaviour of the mode analysis is almost not visible.

Using the same material sandwich, but this time for a microstrip waveguide, a new series of quasi-electrostatic simulations was performed. The geometry used for the simulations consists of a perfect electric conductor as ground plane and a 200 µm wide perfect conducting strip on top of the same three layers that filled up the parallel-plate. Figure 3.10 shows the results for the microstrip capacitance extracted from the simulations. To compare these results to the parallel-plate model, the effective dielectric constant [2] of the microstrip is cal-

[2] The term *effective dielectric constant* (ϵ_{eff}) is used here for both the parallel-plate waveguide as for the microstrip. It can be interpreted as the dielectric constant of a homogeneous medium that replaces all dielectric layers of a waveguide. In the case of the parallel-plate filled with multiple dielectric layers, these layers can be replaced with one dielectric with dielectric constant ϵ_{eff}. For a microstrip, which is an open waveguide, the air above the strip needs to be taken into account and is also replaced by the homogeneous medium.

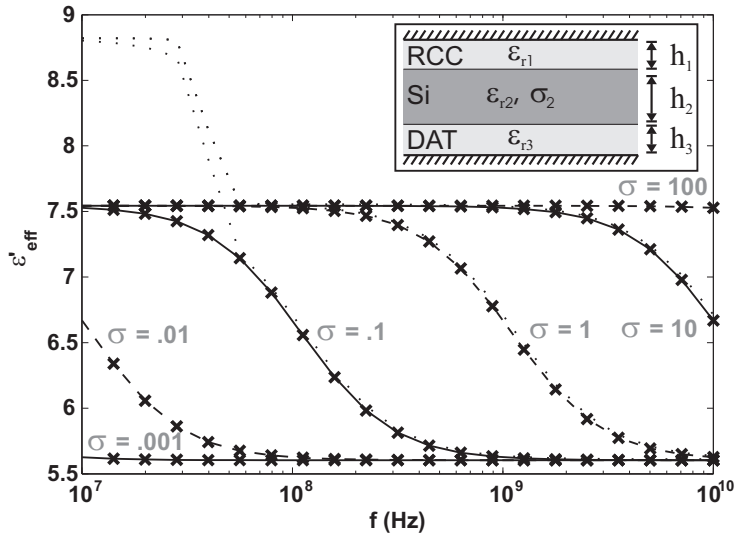


Figure 3.8: Comparison of the simulation results for the parallel-plate with formula (3.40) for the real part of the effective dielectric constant. (—— & - - - -) analytical model; (·····) mode analysis; (✖) quasi-static simulation

culated using the material sandwich as a substrate. First the effective dielectric constant of the substrate is obtained using equation (3.40). This value is then used to calculate the effective dielectric constant of the microstrip, using the following formulae [60].

$$\epsilon_{r,eff} = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2} F \tag{3.47}$$

$$F = \begin{cases} \frac{1}{1.71}(1 + 12\frac{h}{w})^{-\frac{1}{2}} + 0.04(1 - \frac{w}{h})^2 & (\frac{w}{h} \leq 1) \\ \frac{1}{1.71}(1 + 12\frac{h}{w})^{-\frac{1}{2}} & (\frac{w}{h} \geq 1) \end{cases} \tag{3.48}$$

As long as the semiconductor acts as a dielectric, the error between the parallel-plate approximation and the simulation is less than one percent. However, when the conductivity increases, the parallel-plate model fails to correctly predict the effective dielectric constant for the slow-wave mode. This can be explained by looking at the potential distribution. For the parallel-plate waveguide in slow-wave mode, when the semiconductor is regarded as a good conductor, the voltage is distributed inversely proportional to the dielectric constant between the two dielectric layers (layers 1 and 3 in figure 3.6). The semiconductor is held at a fixed potential. The potential distribution for the microstrip

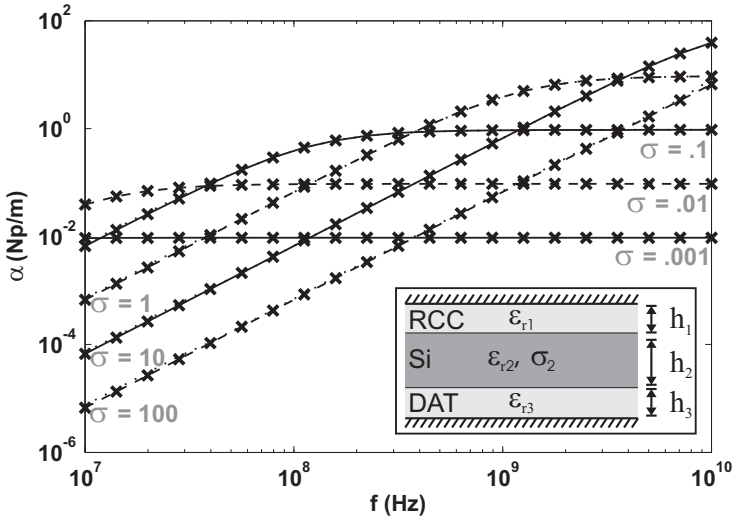


Figure 3.9: Comparison of the simulation results for the parallel-plate with formula (3.45) for the attenuation constant. (—— & - - - -) analytical model; (·····) mode analysis; (✖) quasi-static simulation

in slow-wave mode is slightly different. Since the potential of the semiconductor is again fixed, the lower dielectric layer acts as a parallel-plate capacitor between the ground layer and the semiconductor. The upper dielectric layer can be seen as a microstrip capacitor with the semiconductor as ground layer. To verify this, the total capacitance is calculated as the microstrip capacitance C_{MS} in series with the parallel-plate capacitance C_{PP}.

$$\frac{1}{C_{TOT}} = \frac{1}{C_{MS}\left(w, h_1, \epsilon_{r1}\right)} + \frac{1}{C_{PP}\left(w_{geom}, h_3, \epsilon_{r3}\right)} \tag{3.49}$$

Here, w_{geom} is the total width of the simulation geometry. Using this formula, the total capacitance is 337.3 pF, which is in good agreement with the slow-wave capacitance of the quasi-static simulation (338.5 pF). Although similar propagation modes are present for the multilayer microstrip waveguide, it cannot be described accurately by the models based on the parallel-plate waveguide.

3.2 The multilayer microstrip

As illustrated by the simulation results in the previous section, the parallel-plate approximation is not valid for microstrips when the width of the strip becomes comparable to the height of the substrate. Dedicated models that

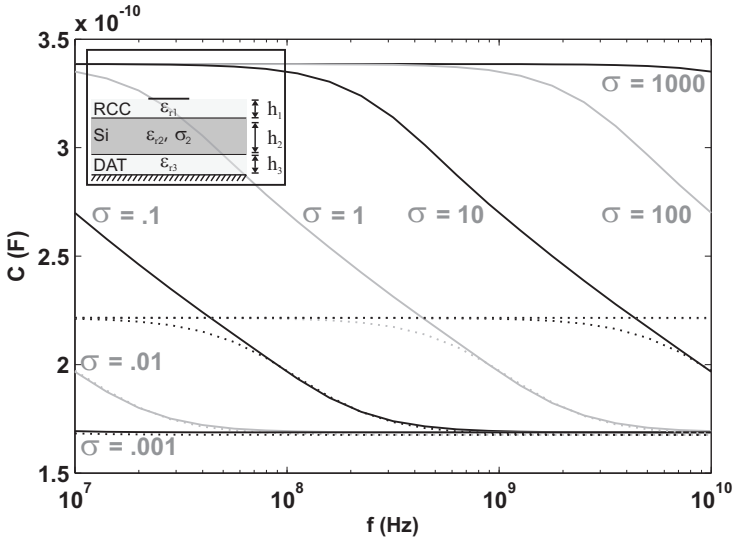


Figure 3.10: Quasi-static simulation results for the capacitance of the microstrip geometry. (——) quasi-static simulation; (·····) parallel-plate approximation

take into account the finite dimensions of the conductors are needed to accurately describe the behaviour of multilayer substrates with one or more conductors. Several numerical methods were applied to microstrips and coplanar waveguides on multilayer substrates, ranging from mode matching techniques [61] and the spectral domain approach (SDA) [62] to complete full-wave analysis by the method of moments (MoM) [63], the finite-difference time domain method (FDTD) [64], or the finite-element method (FEM) [65, 66]. These models are suitable for a large range of geometries, however they often require complex preprocessing steps to set up the calculations. This makes them less suited for integration with fast circuit simulators, where large and complex layouts need to be evaluated quickly. The focus here is on simple approximations that can be implemented in existing models and simulators, without sacrificing too much on accuracy. Before looking at the details of these approximations, a general, full-wave technique is studied to show the physical background behind the numerical methods.

3.2.1 Literature

Before looking at the different models, a comparison between the propagation modes of the parallel-plate waveguide and the multilayer microstrip is made. While Hasegawa et al. give a very good description of the propagation charac-

teristics of a microstrip on a $Si - SiO_2$ system, the proposed formulae are only valid for thin dielectric layers ($\epsilon_2 h_1 \ll \epsilon_1 h_2$) and in the wide-strip limit. A more accurate quantitative representation of the three propagation regions and the transitions in between, requires a full-wave analysis. The spectral domain approach (SDA) covers a wide range of techniques that offer simple and fast full-wave methods for multiconductor structures on multilayer substrates by applying the Fourier transform to the field quantities [62], reducing the partial differential equations to ordinary ones. The SDA method used by Gilb et al. is based on the calculation of the current density on the conductors by applying Galerkin's method to the dyadic Green's functions [67]. Because of the complex permittivity of the substrate layers, these functions are now also complex, leading to two equations for the real and imaginary part of the propagation constant. The results obtained by this method confirm the conclusion based on the parallel-plate waveguide, but reveal that narrow microstrips show a larger slow-wave region since more of the fields are contained in the air and in the upper substrate, reducing the value of the effective dielectric constant that is achieved in the slow-wave region. Thus, a structure with a smaller conductor width enters the slow-wave region earlier and transitions to the skin effect later.

The first analysis, performed by Plaza et al. [63], follows a quasi-TM approach for the computation of the propagation constant of the fundamental mode in planar transmission lines with non-perfect conductors printed on layered dielectric and semiconducting substrates. The transmission line model is based on the per-unit-length shunt complex capacitance and the per-unit-length series complex inductance and requires the consistent definition of the line voltage and current. When using equivalent circuits to describe the propagation characteristics of any waveguide, a correct definition of the line voltage and current is necessary to preserve the physical meaning of the transmission line parameters and to maintain compatibility with the usual concept of complex power. Plaza et al. first define the line voltage based on the quasi-static electric potential and derive the line current from this definition and the expression for the complex power.

$$P = VI^* \tag{3.50}$$

The determination of the transmission line parameters requires the calculation of the quasi-static electric potential and the longitudinal electric current density in the line. The integral equation for the longitudinal current density is solved by a hybrid technique that uses the method of lines (MoL) to compute the quasi-static electric potential and the spatial Green's function for the magnetic potential, and combines this with the method of moments (MoM) to finally obtain the unknown current density. This way the numerical difficulties associated with the root-searching process in the complex plane, typical for the eigenvalue problem of the full-wave propagation system, are avoided.

By limiting the frequency range to assure that $\lambda \gg h$, where h is the

distance between the centre conductor and the ground plane, the average values of the longitudinal fields (in the propagation direction Z-axis) are much smaller than the transverse components (normal to Z). Accordingly, the term $-j\omega\mu_0 H_z$ from Faraday's law of induction can be neglected in the calculation of the transverse field $\mathbf{E_t}$. Although the longitudinal electric field is also smaller than the average transverse electric field, the term σE_z is relevant because of the possible high values of the electric conductivity of the semiconducting layers. The longitudinal electric current in the substrate must be included together with the longitudinal electric current inside the non-perfect metallic conductors to accurately compute the transverse magnetic field $\mathbf{H_t}$ as well as the longitudinal ohmic losses. By neglecting the transverse electric field inside the metallic conductors, the conventional quasi-TEM approach remains valid for computing the transverse electric field in the whole line.

$$\nabla_t \times \mathbf{E_t} = 0 \tag{3.51}$$

$$\mathbf{E_t} = -\nabla_t \phi \tag{3.52}$$

and thus inside each homogeneous layer

$$\nabla_t^2 \phi = 0 \tag{3.53}$$

The following magnetostatic approximation is used to calculate $\mathbf{H_t}$, including the effect of the longitudinal (ohmic) currents.

$$\nabla_t \times \mathbf{H_t} = \sigma \mathbf{E_z} \tag{3.54}$$

Under the quasi-TM assumption $\nabla_t \cdot \mathbf{H_t} = 0$, the transverse magnetic field can be related to the vector potential as

$$\hat{\mathbf{z}} \times \nabla_t A_z = -\mu_0 \mathbf{H_t} \tag{3.55}$$

where $\hat{\mathbf{z}}$ is the unit vector along the Z-axis. Finally, from (3.54) and (3.55), the following equation is found for the Z-component of the vector potential.

$$\nabla_t^2 A_z = -\mu_0 \sigma E_z = -\mu_0 J_z \tag{3.56}$$

Since both A_z and E_z are unknown, an additional equation linking these variables is required. For time-varying magnetic fields, a scalar potential can only be defined if the partial time differential of the vector potential A is added to the electric field to generate a conservative field.

$$\mathbf{E_z} + \frac{\delta \mathbf{A_z}}{\delta t} = -\nabla_z \phi \tag{3.57}$$

Which, for the assumed implicit field dependence $\exp(-j\gamma z + j\omega t)$ leads to

$$E_z = -j\omega A_z + j\gamma\phi. \tag{3.58}$$

The quasi-TM approach can be summarized by equations (3.53), (3.56), and (3.58). Since the propagation constant γ in (3.58) is indeed unknown, only normalized functions A_z/γ, E_z/γ, or J_z/γ can be obtained from (3.56) and (3.58). According to Plaza et al., solving for J_z/γ is the best option in the case of non-perfect metallic conductors. This leads to an integral equation for J_z/γ.

$$\frac{J_z(\mathbf{r})/\gamma}{\sigma(\mathbf{r})} = j\omega\mu_0 \int_S G(\mathbf{r},\mathbf{r}')\, J_z(\mathbf{r})/\gamma \; \mathrm{d}S + j\phi(\mathbf{r}) \tag{3.59}$$

where $G(\mathbf{r},\mathbf{r}')$ is the Green's function corresponding to (3.56). This integral equation is solved by a mixed approach that combines the MoL with the MoM.

As a result, the quasi-static electric potential and the longitudinal electric current density are obtained. The voltage V is then defined as the quasi-static electric potential in the centre conductor and as a consequence the line current can be derived from (3.50).

$$I = I_c + \frac{1}{V^*} \int_{S(s)} J_z \phi^* \mathrm{d}S \tag{3.60}$$

where $S(s)$ is the cross section corresponding to the conductive layers and I_c is the current associated to the centre conductor. Once the voltage and current have been defined, the proper expressions for the complex series inductance $\hat{L}$ and shunt capacitance $\hat{C}$ per-unit-length can be obtained enforcing the telegrapher's equations.

$$j\gamma V = j\omega \hat{L} I \tag{3.61}$$

$$j\gamma I = j\omega \hat{C} V \tag{3.62}$$

This approach is both accurate and flexible as it incorporates non-perfect conductors with finite thickness and can be used for microstrip and coplanar waveguides on an arbitrary number of dielectric and semiconducting layers. However, the lack of closed-form expressions and the issues with for example setting up a good discretization for the method of moments make this approach less adequate for practical use in a design environment.

The desire to develop a fast and accurate model suitable for CAD implementation that takes into account all three modes of propagation on a slow-wave microstrip line with conductor loss was the motivation for Verma et al. [68] to propose a more simple technique. The formulation is based on the single-layer reduction (SLR) process, which converts a multilayer microstrip geometry to a single-layer microstrip structure (figure 3.11). The single-layer substrate has an equivalent relative permittivity ($\epsilon_{r,eq}$) and an equivalent loss tangent ($\tan\delta_{eq}$). The thickness of the equivalent single-layer substrate is the total thickness between the ground plane and the strip conductor of the original structure, while the width of the central strip is kept unchanged.

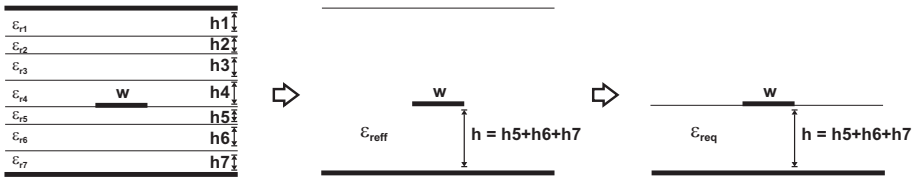


Figure 3.11: Principle of the single-layer reduction model proposed by Verma et al. The multilayer substrate is first reduced to a homogeneous medium with dielectric constant ϵ_{eff}, which is then transformed into the equivalent dielectric constant of the single-layer substrate

This transformation occurs in two steps. The first step converts the multilayer medium of the microstrip into a homogeneous medium completely surrounding the microstrip. This is equal to the concept of the effective dielectric constant for a classical microstrip structure and so the complex relative permittivity of the homogeneous medium is referred to as $\epsilon^{\star}_{reff}$. This effective dielectric constant is converted to the equivalent relative permittivity of the substrate below the microstrip using the inverse of the classical formula for microstrip analysis (equation (3.47)).

The effective complex permittivity in the first step is computed from the complex line capacitance that is obtained by a variational method [69]. Consider an infinitely thin microstrip line with width w and substrate height h. The line capacitance of the strip can be defined as the square of the total charge of the strip divided by the stored energy on the strip.

$$\frac{1}{C} = \frac{1}{Q^2} \int_{-w/2}^{w/2} f(x)\phi(x,h)dx \tag{3.63}$$

$$Q = \int_{-w/2}^{w/2} f(x)dx \tag{3.64}$$

Here, $f(x)$ and $\phi(x,h)$ are respectively the charge density and the electric potential on the strip. The variational method aims to minimize this expression by finding a suitable trial function for the charge density $f(x)$. Solving the Poisson's equation using the Green's function is more convenient in the Fourier domain, thus the expression for the line capacitance is Fourier transformed as well.

$$\frac{1}{C} = \frac{1}{\pi} \int_0^{\infty} \left| \frac{\tilde{f}(\beta)}{Q} \right|^2 \frac{1}{\beta Y} \, \mathrm{d}\beta \tag{3.65}$$

With β being the Fourier variable, $\tilde{f}(\beta)$ is the Fourier transform of $f(x)$. The admittance parameter Y is related to the Green's function for the multilayer structure.

Since the charge density distribution $f(x)$ is still unknown, a reasonable trial function has to be chosen. The charge density on an infinitely thin conductor strip in free space has been calculated based on electrostatic theory [70], and reveals the rapid increase of the charge density near the edge of the strip.

$$f(x) = \begin{cases} \left[1 - \left(\dfrac{2x}{w}\right)^2\right]^{-\frac{1}{2}} & -\dfrac{w}{2} \leq x \leq \dfrac{w}{2} \\ 0 & \text{elsewhere} \end{cases} \tag{3.66}$$

where w is the width of the strip. A trial function of this type would be a logical choice for the microstrip. It is an advantage of the variational expression that the accuracy of the calculated value is relatively insensitive to the choice of the trial function. Since the approximate line capacitance obtained by this method is always smaller than the exact value, a trial function resulting in a larger line capacitance is a more appropriate trial function. As found by Yamashita [71], the following trail functions offers a good compromise between computing time and accuracy.

$$f(x) = \begin{cases} 1 + \left|\dfrac{2x}{w}\right|^3 & -\dfrac{w}{2} \leq x \leq \dfrac{w}{2} \\ 0 & \text{elsewhere} \end{cases} \tag{3.67}$$

Finally, the Fourier transform of this trial function is

$$\begin{aligned} \frac{\tilde{f}(\beta)}{Q} &= \frac{8}{5}\frac{\sin(\beta w/2)}{\beta w/2} \\ &\quad + \frac{12}{5(\beta w/2)^2}\left(\cos(\beta w/2) - \frac{2\sin(\beta w/2)}{\beta w/2} + \frac{\sin^2(\beta w/4)}{(\beta w/4)^2}\right) \end{aligned} \tag{3.68}$$

The admittance parameter Y can be calculated using the transverse transmission line method. This very simple and clever method for the calculation of the spectral Green's function was introduced by Crampagne et al. [72]. The multilayer substrate is regarded as a series of transmission lines, where the height h_i of each layer is the length of the line and the dielectric constant is used as the characteristic admittance Y_0^i of the transmission line. The series can be terminated by a short-circuit (ground plane or shielding), an open circuit (air interface) or by a matched charge (infinitely long dielectric). This results in a general theory which is independent of the number of dielectric layers and the location of the conductor strip in the layer stack. The total admittance can be calculated by iterating the following formula.

$$Y_{in}^i = Y_0^i \frac{Y_{in}^{i+1} + Y_0^i \tanh(\beta h_i)}{Y_0^i + Y_{in}^{i+1} \tanh(\beta h_i)} \tag{3.69}$$

where Y_{in}^{i} denotes the input admittance at the interface between layer i and $i-1$. The indexing of the layers starts at the signal conductor and progresses towards the outer boundaries. For example, a single-layer microstrip with dielectric constant ϵ_r and height h above a perfect conducting ground plane ($Y_{in} = \infty$), leads to the following admittance parameter.

$$Y = 1 + \frac{\epsilon_r}{\tanh \beta h} \tag{3.70}$$

Each substrate layer is characterised by a complex relative permittivity, that can be written as

$$\epsilon_{ri}^{\star} = \epsilon_{ri}' - j\frac{\sigma_i}{\omega\epsilon_0} \qquad \text{or} \qquad \epsilon_{ri}^{\star} = \epsilon_{ri}' - j\epsilon_{ri}' \tan\delta_i \tag{3.71}$$

where ϵ_{ri}' is the real relative permittivity, σ_i the conductivity and $\tan\delta_i$ is the loss tangent of each dielectric layer. The complex effective dielectric constant of the multilayered slow-wave microstrip is obtained from the ratio of the complex line capacitance C to the line capacitance C_0 of the structure when all the layers are replaced by air.

$$\epsilon_{reff}^{\star} = \epsilon_{reff}' - j\epsilon_{reff}'' = \frac{C}{C_0} \tag{3.72}$$

From this value, the complex characteristic impedance can be obtained.

$$Z = \frac{Z_0}{\sqrt{\epsilon_{reff}^{\star}}} \tag{3.73}$$

where Z_0 is the characteristic impedance of the microstrip on an air substrate.

The effect of the conductor thickness t on the effective relative permittivity is accounted for by the following expression.

$$\epsilon_{reff}'(\epsilon_{r1}, \epsilon_{r2}, \ldots, w, h_1, h_2, \ldots, t) = \epsilon_{reff}'(\epsilon_{r1}, \epsilon_{r2}, \ldots, w, h_1, h_2, \ldots, t=0) - \frac{\left(\epsilon_{req}' - 1\right)}{4.6}\frac{t/h}{\sqrt{(w/h)}} \tag{3.74}$$

where ϵ_{req}' of the equivalent single-layer substrate is obtained from equation (3.47) and h is the total thickness of the substrate. The conductive and dielectric loss of the microstrip structure can now be calculated based on the effective dielectric constant (see 3.2.2 for detailed formulae).

Verma et al. show that the SLR formulation gives very good results for the slow-wave and dielectric region, but fails to predict the transition to the skin effect mode. In this region the TEM nature of the mode propagation breaks down and the TM nature becomes important. Therefore, the SLR formulation requires some modifications so that it is valid in all three regions.

In order to differentiate between the propagation modes, Verma et al. use the value of the conductivity of the semiconducting layer. At the beginning of the transition from the slow-wave mode to the skin effect region, a local minimum of the attenuation constant is reached. The value of the conductivity (σ_{min}) was calculated for a two-layer structure by Hasegawa et al. [54] and verified by Gilb et al. [67] by a full-wave analysis. The onset of the skin effect region was at the same time defined as the conductivity (σ_{max}) for which the depth of penetration in the semiconducting layer becomes equal to its thickness.

$$\sigma_{min} = \sqrt{\frac{3\epsilon_0\epsilon_s}{\mu_0 h_1 h_s}} \tag{3.75}$$

$$\sigma_{max} = \frac{1}{\pi f \mu_0 h_s^2} \tag{3.76}$$

The improved version of the SLR formulation uses the standard formulation from $\sigma = 0$ to $\sigma = \sigma_{min}$, corresponding to the slow-wave and dielectric propagation modes. Between σ_{min} and σ_{max}, the dielectric loss is calculated using a normalised conductivity by dividing the conductivity of the semiconducting layer by σ_{max}. The calculation of the effective dielectric constant does not change. Finally, in the skin effect region where $\sigma \geq \sigma_{max}$, the thickness of the semiconducting layer is replaced by the skin depth in this layer.

$$h_{s\,eff} = \delta_{Si} \tag{3.77}$$

Based on the effective complex permittivity, the attenuation constant and the characteristic impedance calculated by the improved SLR formulation, a circuit model consisting of the per-unit-length resistance, conductance, inductance and capacitance can be derived to described the propagation behaviour of the microstrip structure.

Verma et al. fail to extend this improved method to an arbitrary number of layers and admit that the "*treatment of the TM mode by using the TEM mode is only phenomenological*". The increasing longitudinal currents in the conductive regions at the onset of the skin effect region cause a sharp rise in resistance and a similar drop in inductance. Although the per-unit-length shunt impedance parameters, the capacitance and the conductance, are predicted accurately by the SLR method over a wide frequency range, the frequency dependent behaviour of the inductance and the resistance is not incorporated in a coherent and physical manner.

A more consistent approach for the series impedance parameters can be found in [73]. Weisshaar et al. derive closed-form expressions for the resistance and inductance per-unit-length using a complex image approach [74]. This technique places image conductors at a frequency-dependent complex depth below the interconnects. A generalized surface impedance boundary condition, located at the interface between the dielectric and conductive layer, is

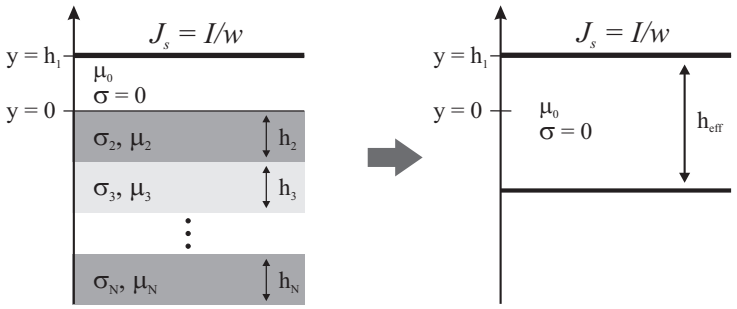


Figure 3.12: Conversion of a multilayer conductive substrate into an equivalent non-conducting layer with complex thickness h_{eff}

calculated by a simple recursive input impedance formulation. This is again based on the transverse resonance technique, similar to the calculation of the admittance parameter above.

A first order approximation of the effective depth is determined by calculating the complex inductance per-unit-length for a perfectly conducting plate of width w above a multilayer conductive substrate. For the one-dimensional geometry shown in Figure 3.12, the magnetic vector potential in the non-conducting top layer becomes (see [73] for details)

$$A_z(y) = \mu_0 \frac{I}{w}\left(y + \frac{Z_s}{j\omega\mu_0}\right) \qquad (0 \le y \le h_1) \tag{3.78}$$

from which the complex inductance is derived as

$$L^{\star}(\omega) = L(\omega) - j\frac{R(\omega)}{\omega} = \frac{\mu_0}{w}\left(h_1 + \frac{Z_s}{j\omega\mu_0}\right) \tag{3.79}$$

where I is the total current on the conductor and h_1 the height of the upper non-conducting layer. The surface impedance Z_s can be determined as the input impedance of the equivalent problem of cascaded transmission lines, with a characteristic impedance equal to the intrinsic impedance η_i and a propagation constant γ_i.

$$\eta_i = \frac{j\omega\mu_i}{\gamma_i} = \frac{\gamma_i}{\sigma_i} \tag{3.80}$$

$$\gamma_i = \sqrt{j\omega\mu_i\sigma_i} = \frac{1+j}{\delta_i} \tag{3.81}$$

where δ_i is the skin depth of layer i. For a general multilayer substrate, the input impedance is obtained by recursive application of the following expression.

$$Z_{in}^{i} = Z_0^{i}\frac{Z_{in}^{i+1} + Z_0^{i}\tanh(\gamma_i h_i)}{Z_0^{i} + Z_{in}^{i+1}\tanh(\gamma_i h_i)} \tag{3.82}$$

Z_{in}^{i} is the input impedance at the interface between layer i and $i-1$ and h_i is the thickness of layer i. At the lowest layer, the boundary condition is either $Z_{in} = 0$ for a perfectly conducting plane or $Z_{in} \to \infty$ for a non-conducting semi-infinite medium. Weisshaar et al. assume a series of conductive layers for the calculation of the surface impedance. However, the final layer above the ground plane in the geometry of Figure 3.13 is non-conductive.

To adapt the expression of the surface impedance, the origin of expressions for the characteristic impedance ((3.80)) and the propagation constant ((3.81)) needs to be explained [59]. For a plane wave in a general lossy medium, the wave equation derived from Maxwell's curl equations results in

$$\nabla^2 \mathbf{E} + \omega^2 \mu\epsilon \left(1 - j\frac{\sigma}{\omega\epsilon}\right) \mathbf{E} = 0. \tag{3.83}$$

A complex propagation constant and a wave impedance, relating the magnetic and electric fields, can be defined for the medium.

$$\gamma = j\omega\sqrt{\mu\epsilon}\sqrt{1 - j\frac{\sigma}{\omega\epsilon}} \tag{3.84}$$

$$\eta = \frac{j\omega\mu}{\gamma} \tag{3.85}$$

For a good conductor, as in the case considered by Weisshaar et al., the conductive current is much greater than the displacement current or $\sigma \gg \omega\epsilon$. This leads to the following approximation for the propagation constant.

$$\gamma \approx j\omega\sqrt{\mu\epsilon}\sqrt{\frac{\sigma}{j\omega\epsilon}} = (1+j)\sqrt{\frac{\omega\mu\sigma}{2}} \tag{3.86}$$

For a lossless dielectric medium, the conductivity $\sigma = 0$ and thus

$$\gamma = j\omega\sqrt{\mu\epsilon} \tag{3.87}$$

$$\eta = \frac{j\omega\mu}{\gamma} = \sqrt{\frac{\mu}{\epsilon}}. \tag{3.88}$$

Taking into account the perfect conducting ground plane ($Z_{in} = 0$), the input impedance for the lowest, non-conducting layer in Figure 3.13 becomes

$$Z_{in,ll} = \sqrt{\frac{\mu_0}{\epsilon_0\epsilon_{r3}}} \tanh\left(j\omega\sqrt{\mu_0\epsilon_0\epsilon_{r3}}h_3\right) \approx j\omega\mu h_3 \tag{3.89}$$

Since the height of the die bond adhesive layer is small, the final approximation introduces no loss of accuracy (the error at 100 GHz is less than 0.2%). The boundary condition for a non-conducting semi-infinite medium ($Z_{in} \to \infty$) can also be derived from this expression.

The term between brackets in (3.79) can be interpreted as an effective complex height of a parallel-plate transmission line, filled with a non-conductive, non-magnetic material.

$$h_{eff} = h_1 + \frac{1}{j\omega\mu_0}\frac{j\omega\mu_2}{\gamma_2}\frac{Z_{in}^2}{Z_0^2} = h_1 + (1-j)\,\frac{\delta_2}{2}\frac{\mu_2}{\mu_0}\frac{Z_{in}^2}{Z_0^2} \tag{3.90}$$

The concept of the single-layer reduction and the introduction of the effective complex height make it possible to accurately describe the behaviour of the multilayer microstrip in a concise way. The implementation can be readily expanded to more layers; however, the transverse resonance principle, which is the basis of both implementations, becomes less accurate when the number of layers increases. The big advantage over other, full-wave based models is that it can be implemented using the existing microstrip design formulae, as will be shown in the next section.

3.2.2 Final model

The best compromise between flexibility, speed and accuracy is made by using the model by Verma et al. for the calculation of the effective dielectric constant and the dielectric loss, and the closed-form expressions by Weisshaar et al. for the series impedance parameters. This section shows the implementation of both principles for the calculation of the per-unit-length parameters of the multilayer microstrip shown in figure 3.13, based on well-known formulae for the classic microstrip. The final model is not optimised to reach the highest accuracy, but only intended to show that these simple approximations can lead to precise result and correctly reflect the behaviour of the multilayer microstrip. The model was implemented in Matlab and the complete code listing can be found in appendix C.

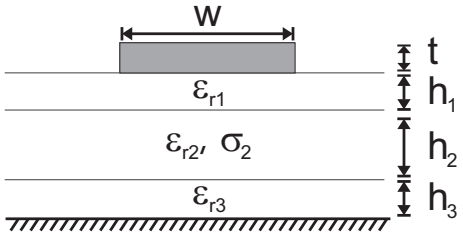


Figure 3.13: Geometry for a trace running on top of an embedded component. Layer 1 is the RCC, layer 2 is the silicon and layer 3 is the die bond adhesive

The first step is to calculate the trial function for the variational expression based on equation (3.68). Before the capacitance can be calculated using this

trial function, the admittance parameter for the geometry in figure 3.13 needs to be derived. Starting from the lowest layer, the die bond layer, the first iteration step leads to the following admittance.

$$Y_{in}^3 = \frac{\epsilon_{r3}}{\tanh \beta h_3} \tag{3.91}$$

The next layer is the silicon chip.

$$Y_{in}^2 = \epsilon_{r2} \frac{Y_{in}^3 + \epsilon_{r2} \tanh \beta h_2}{\epsilon_{r2} + Y_{in}^3 \tanh \beta h_2} \tag{3.92}$$

$$= \epsilon_{r2} \frac{\epsilon_{r3} + \epsilon_{r2} \tanh \beta h_2 \tanh \beta h_3}{\epsilon_{r2} \tanh \beta h_3 + \epsilon_{r3} \tanh \beta h_2} \tag{3.93}$$

The final iteration step includes the effect of the RCC layer.

$$Y_{in}^1 = \epsilon_{r1} \frac{Y_{in}^2 + \epsilon_{r1} \tanh \beta h_1}{\epsilon_{r1} + Y_{in}^2 \tanh \beta h_1} \tag{3.94}$$

The admittance parameter Y is the shunt connection of the admittance of the substrate below the strip and the admittance of the air above the strip, which can be seen as an infinitely thick dielectric layer ($Y_{in} = 1$).

$$Y = Y_{in}^1 + 1 \tag{3.95}$$

To calculate the capacitance when all the layers are replaced by air, the relative dielectric constants are all set to 1. The integral in equation (3.65) is approximated using numerical integration (adaptive Gauss-Kronrod quadrature). The capacitance of the multilayer microstrip structure is computed by substituting the following expressions for the dielectric constants.

$$\epsilon_{r1} = \epsilon'_{r1} (1 - j \tan \delta_1) \tag{3.96}$$

$$\epsilon_{r2} = \epsilon'_{r2} - j \frac{\sigma_2}{2\pi f \epsilon_0} \tag{3.97}$$

$$\epsilon_{r3} = \epsilon'_{r3} (1 - j \tan \delta_3) \tag{3.98}$$

The effective dielectric constant is derived from the ratio of the capacitance with and without dielectrics and compensated for the track thickness of the microstrip. The characteristic impedance of the multilayer microstrip is calculated by inserting the effective dielectric constant in the classic formulae from [75].

$$Z_0 = \frac{60}{\sqrt{\epsilon'_{reff}}} \ln \left(\frac{8}{w_e/h} + 0.25 \frac{w_e}{h} \right) \qquad \frac{w}{h} \leq 1 \tag{3.99}$$

$$Z_0 = \frac{120\pi}{\sqrt{\epsilon'_{reff}}} \left(\frac{w_e}{h} + 1.393 + 0.667 \ln \left(\frac{w_e}{h} + 1.444 \right) \right)^{-1} \qquad \frac{w}{h} \geq 1 \tag{3.100}$$

where

$$\frac{w_e}{h} = \frac{w}{h} + \frac{1.25}{\pi}\frac{t}{h}\left(1 + \ln\frac{4\pi w}{t}\right) \qquad \frac{w}{h} \leq \frac{1}{2\pi} \tag{3.101}$$

$$\frac{w_e}{h} = \frac{w}{h} + \frac{1.25}{\pi}\frac{t}{h}\left(1 + \ln\frac{2h}{t}\right) \qquad \frac{w}{h} \geq \frac{1}{2\pi} \tag{3.102}$$

The conductive and dielectric loss are calculated based on the formulae proposed by Verma et al. The formula for the conductive loss, α_c, is derived from the Wheeler incremental inductance rule, where the loss is proportional to the change in characteristic impedance when all conductor walls are receded by $\delta_{Cu}/2$, as explained in [59].

$$\delta_{Cu} = \frac{1}{\sqrt{\pi f \mu_0 \sigma_{Cu}}} \tag{3.103}$$

$$\alpha_c = \frac{\pi f}{c}\sqrt{\epsilon'_{reff}}\frac{Z_0\left(\epsilon = 1, w - \delta_{Cu}, h + \delta_{Cu}/2, t - \delta_{Cu}\right) - Z_0\left(\epsilon = 1, w, h, t\right)}{Z_0\left(\epsilon = 1, w, h, t\right)} \tag{3.104}$$

$$\alpha_d = \frac{\pi f}{c}\frac{\epsilon''_{reff}}{\sqrt{\epsilon'_{reff}}} \tag{3.105}$$

$$\alpha = \alpha_c + \alpha_d \tag{3.106}$$

Using the characteristic impedance, the effective dielectric constant and the dielectric loss, the shunt impedance parameters can be derived. The series impedance parameters are calculated by introducing the effective height for high-conductivity silicon into the closed-form formula by Wheeler [60] for the inductance, with compensation for the finite strip thickness.

$$L^\star(\omega) = L(\omega) - j\frac{R(\omega)}{\omega} \tag{3.107}$$

$$= \frac{\mu_0}{4\pi}\ln\left\{1 + 32\left(\frac{h_{eff}}{w_{eff}}\right)^2\left[1 + \sqrt{1 + \left(\frac{\pi}{8}\frac{w_{eff}}{h_{eff}}\right)^2}\right]\right\} \tag{3.108}$$

$$w_{eff} = w + \frac{t}{\pi}\ln\frac{4\exp(1)}{\sqrt{\left(\frac{t}{h_{eff}}\right)^2 + \frac{1}{\left(\pi\left(\frac{w}{t} + 1.10\right)\right)^2}}} \tag{3.109}$$

The derivation of h_{eff} is similar to the calculation of the admittance parameter Y and is described briefly below.

$$Z_{in}^2 = Z_0^2\frac{Z_{in}^3 + Z_0^2\tanh(\gamma_2 h_2)}{Z_0^2 + Z_{in}^3\tanh(\gamma_2 h_2)} \tag{3.110}$$

Using the definition of the characteristic impedance (3.80) and the propagation constant (3.81), this becomes

$$\frac{Z_{in}^2}{Z_0^2} = \frac{j\omega\mu_0 h_3 + \frac{j\omega\mu_0}{\gamma_2}\tanh\left(\frac{1+j}{\delta_2}h_2\right)}{\frac{j\omega\mu_0}{\gamma_2} + j\omega\mu_0 h_3 \tanh\left(\frac{1+j}{\delta_2}h_2\right)} \tag{3.111}$$

$$= \frac{h_3 + \frac{\delta_2}{1+j}\tanh\left(\frac{1+j}{\delta_2}h_2\right)}{\frac{\delta_2}{1+j} + h_3 \tanh\left(\frac{1+j}{\delta_2}h_2\right)} \tag{3.112}$$

Insert this into (3.90) to obtain the expression for h_{eff}

$$h_{eff} = h_1 + \frac{1-j}{2}\delta_2 \frac{h_3 + \frac{\delta_2}{1+j}\tanh\left(\frac{1+j}{\delta_2}h_2\right)}{\frac{\delta_2}{1+j}\left(1 + h_3\frac{1+j}{\delta_2}\tanh\left(\frac{1+j}{\delta_2}h_2\right)\right)} \tag{3.113}$$

$$= h_1 + \frac{h_3 + \frac{\delta_2}{1+j}\tanh\left(\frac{1+j}{\delta_2}h_2\right)}{1 + h_3\frac{1+j}{\delta_2}\tanh\left(\frac{1+j}{\delta_2}h_2\right)} \tag{3.114}$$

The *internal* inductance L_{int} of the microstrip is again determined using the incremental inductance rule of Wheeler. The resistance obtained using the effective complex height describes the loss in the semiconducting layer ($L^\star$ is only complex because of h_{eff} being complex) and is thus added to the resistance derived from the conductive loss.

$$L_{tot}(\omega) = \Re(L^\star) + L_{int}(\omega) \tag{3.115}$$

$$R_{tot}(\omega) = R_{Si}(\omega) + R_{Cu}(\omega) \tag{3.116}$$

$$= -\omega\,\Im(L^\star) + \sqrt{\left(\frac{1}{wt\sigma_{Cu}}\right)^2 + (2\alpha_c Z_0)^2} \tag{3.117}$$

The squared addition for the conductive resistance better describes the transition from DC tot the skin effect region, according to Johnson et al. [32]. Finally, the shunt admittance parameters are defined.

$$C_{tot}(\omega) = \frac{\sqrt{\epsilon'_{eff}}}{c\,\Re(Z_0)} \tag{3.118}$$

$$G_{tot}(\omega) = \frac{2\alpha_d}{\Re(Z_0)} \tag{3.119}$$

3.2.3 Simulations

The behaviour of the multilayer microstrip is analysed using a finite element method (FEM) 3D electromagnetic simulator (*Comsol Multiphysics*). Two different types of simulations are performed to characterise the propagation modes and verify the different approximations. The first series of simulations consists of a mode analysis on the cross-section of a multilayer microstrip to determine the propagation constant. Next to that, a combined quasi-static electric and magnetic simulation is performed to calculate the per-unit-length shunt and series impedance parameters. Both simulation runs are compared to the proposed model to verify the accuracy and the limitations of the model.

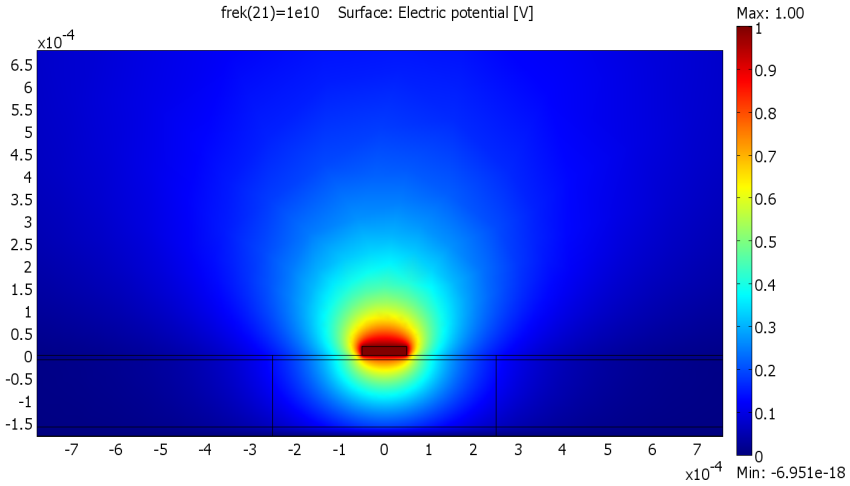


Figure 3.14: Close-up of the geometry for the mode analysis and quasi-static simulations. The colour map shows the potential distribution for the transition region between the dielectric and the skin effect mode ($f = 10\,\text{GHz}$). From the bottom to the top: a 20 µm die attach tape, a 150 µm silicon layer, 10 µm of RCC, the copper trace with a width of 100 µm and a thickness of 20 µm and finally air surrounding the strip. The remaining part of the geometry is not shown for clarity, but is just an extension of the current view.

The simulation geometry for the mode analysis consists of a 5 mm wide and 1 mm high box. The size of the box is chosen to minimize the influence of the outer boundary conditions on the simulation results. All outer boundary conditions consist of perfect magnetic conductors ($\mathbf{n} \times \mathbf{H} = 0$), except for the lower boundary which is a perfect electric conductor ($\mathbf{n} \times \mathbf{E} = 0$) acting as ground plane for the microstrip. The remaining boundaries are continuous. Drawing a three-layer microstrip with finite track thickness, results in five subdomains (Figure 3.14): The die bond adhesive layer (DAT, $\epsilon_r = 3$), the

silicon chip (Silicon, $\epsilon_r = 12.1$, $\sigma = \sigma_2$), the resin covering the chip (RCC, $\epsilon_r = 3.8$), the air above the substrate (Air, $\epsilon_r = 1$) and finally the copper strip itself (Cu, $\sigma = 5.98\text{e}7\,\mathrm{S/m}$). Both dielectric layers are assumed to be lossless ($\tan\delta_1 = \tan\delta_3 = 0$). At high frequencies, the skin depth of the copper becomes very small compared to the thickness of the trace, requiring very dense meshing of the strip conductor. This increases the simulation time, which is avoided by replacing the copper by a hollow domain surrounded by an impedance boundary condition. The propagation constant is obtained by performing a mode analysis on the electric field of a hybrid-mode wave, after inputting the frequency and a starting point for the eigenvalue search algorithm. The simulation is converted to a batch file, which automatically varies the frequency (21 logarithmically spaced points between 100 MHz and 10 GHz) and the conductivity of the silicon ($\sigma_2 = \{0.001, 0.01, 0.1, 1, 10, 100, 1000\}\,\mathrm{S/m}$).

Table 3.1: Different geometries for the multilayer microstrip. All values in μm

w	h_1	h_2	h_3	t
100	10	20	20	20
250	10	20	20	20
100	10	150	20	20
250	10	150	20	20
100	50	20	20	20
250	50	20	20	20
100	50	150	20	20
250	50	150	20	20

Table 3.1 list all the geometrical parameters that were used for the simulations. The values were chosen to reflect the most likely possibilities for chip embedding, in such a way that any inconsistencies would be apparent quickly. The thickness of the die attach tape is kept constant at 20 μm, while the chip thickness and the height of the RCC above the chip are varied from 20 μm to 150 μm and from 10 μm to 50 μm, respectively. The width of the strip was either 100 μm or 250 μm.

Looking at the results from the mode analysis, it is clear that there are quite some discrepancies between the model and the simulations. Figure 3.15 compares the effective dielectric constant obtained from the mode analysis to the value predicted by the single-layer reduction technique of Verma et al. For low conductivity of the silicon and at higher frequencies, the correspondence is reasonably good. At low frequencies, the mode analysis is influenced by the finite dimensions of the simulation geometry and the whole box starts to act as a waveguide. This translates into an increased value of the effective dielectric constant below 500 MHz. A second discrepancy occurs when the conductivity

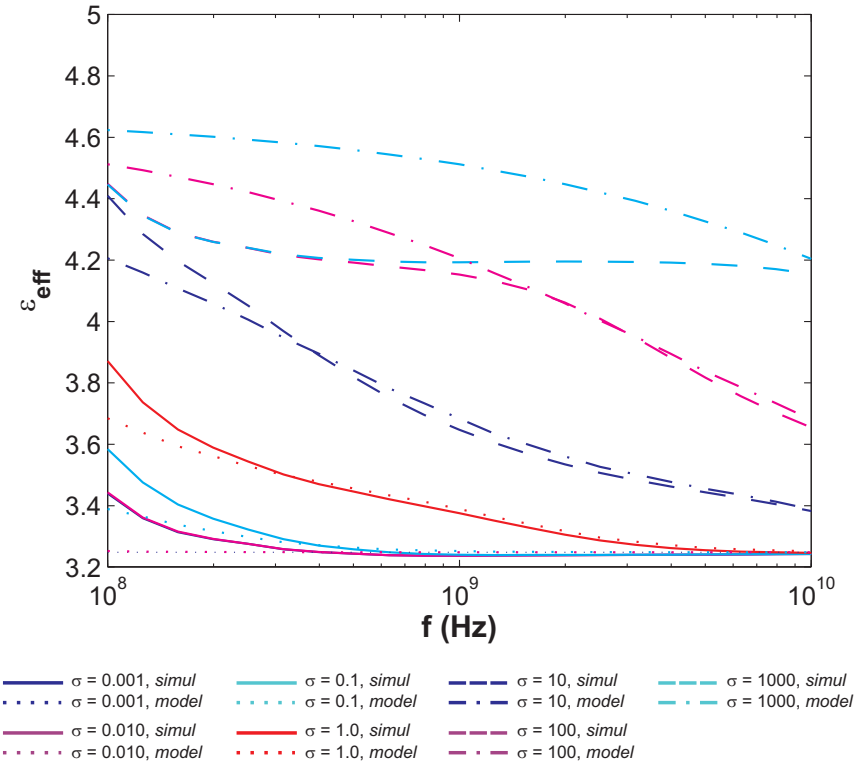


Figure 3.15: Comparison of the effective dielectric constant derived from the mode analysis to ϵ_{eff} predicted by the SLR model of Verma et al. ($w = 250\,\mu\text{m}$, $h_1 = 50\,\mu\text{m}$, $h_2 = 20\,\mu\text{m}$, $h_3 = 20\,\mu\text{m}$ and $t = 20\,\mu\text{m}$)

of the silicon becomes larger than 100 S/m. The effective dielectric constant seems to saturate at a lower value than predicted by the model. This can be explained by looking again at equation (3.49). The capacitance, and thus the effective dielectric constant, is limited by the value of the parallel-plate capacitance between the conductive silicon and the ground layer, which depends on the total width of the simulation geometry. The results can be improved by widening the geometry, however the simulation time rises accordingly. A similar effect can be seen looking at the total loss of the microstrip, obtained from the real part of the propagation constant (figure 3.16). Up to a conductivity of 10 S/m, the model corresponds quite good to the simulations. Above that, the values diverge at low frequencies, but meet up again at higher frequencies.

Before moving to the quasi-static simulations, a more detailed look at what happens for thicker silicon is needed. As stated before, the basic model of Verma

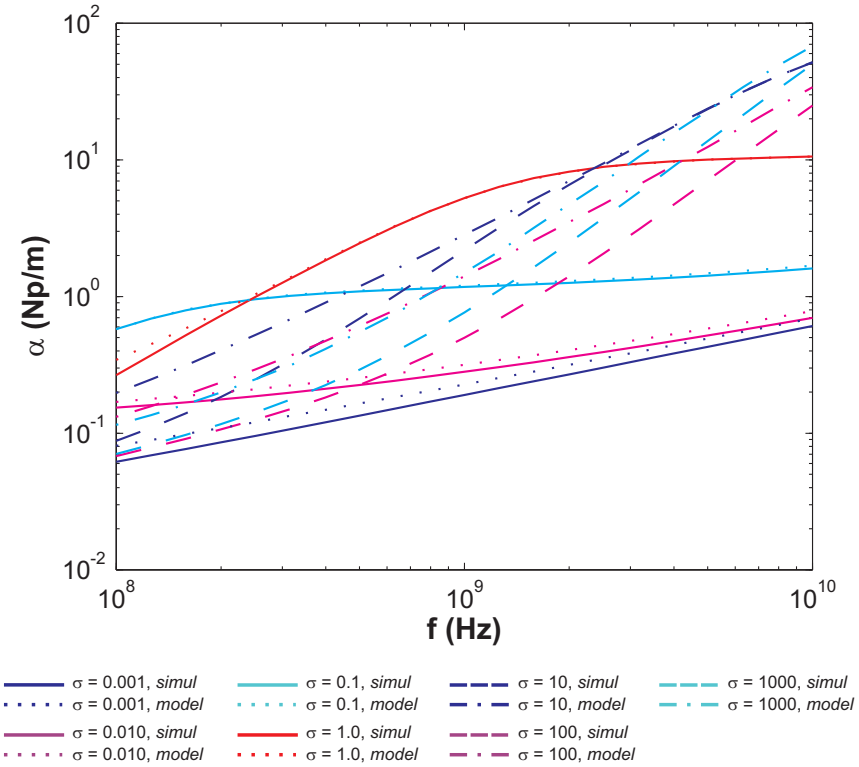


Figure 3.16: Comparison of the total loss derived from the mode analysis to α_{tot} predicted by the SLR model of Verma et al. ($w = 250\,\mu m$, $h_1 = 50\,\mu m$, $h_2 = 150\,\mu m$, $h_3 = 20\,\mu m$ and $t = 20\,\mu m$)

et al. does not take into account the skin effect mode. At 10 GHz, the 150 µm thick silicon is already at the onset of this mode ($f_\delta = 11.3\,GHz$). This can be seen in figure 3.17, where the simulated curve for a conductivity of 1000 S/m starts descending before the 100 S/m curve. This is not reflected by the ϵ_{eff} as calculated with the SLR model, where the curve for the highest conductivity always stays above the rest. The overall offset between the simulation results and the model seems quite large but is only about 5 %.

To avoid the inaccuracies of the mode analysis simulation, a second type of simulations is introduced to directly calculate the per-unit-length RLGC parameters. The approach of the simulations is similar to the method of Plaza et al. [63], which was discussed in section 3.2.1. First the potential distribution of the multilayer microstrip is calculated using a quasi-electrostatic simulation, which automatically produces the capacitance and the conductance. The

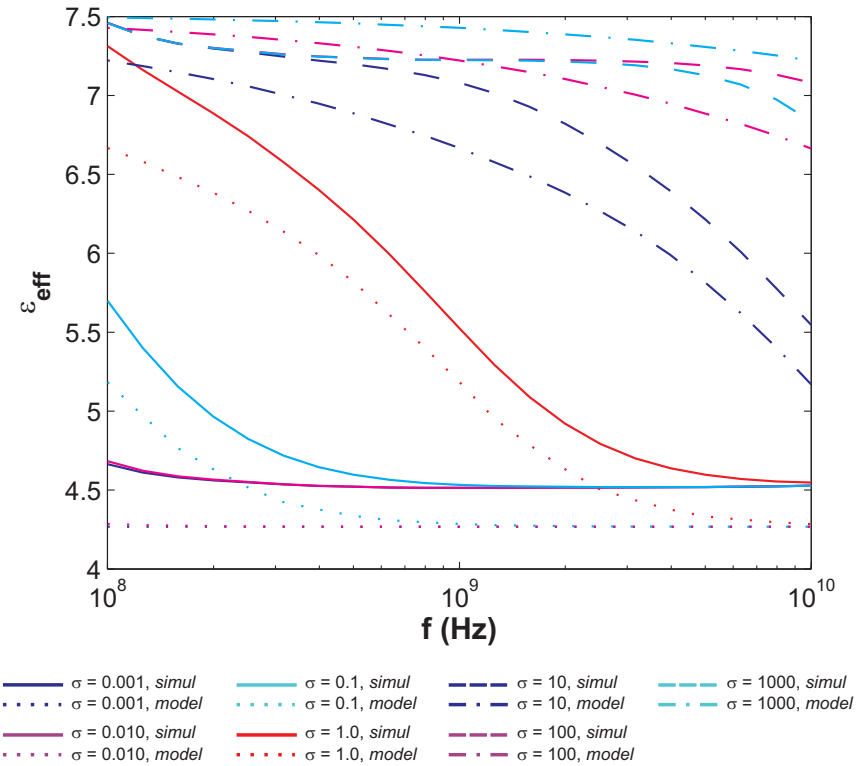


Figure 3.17: Comparison of the effective dielectric constant derived from the mode analysis to ϵ_{eff} predicted by the SLR model of Verma et al. Notice how the dashed blue curve ($\sigma = 1000\,\mathrm{S/m}$) starts decreasing before the pink dashed curve ($\sigma = 100\,\mathrm{S/m}$). ($w = 250\,\mu\mathrm{m}$, $h_1 = 50\,\mu\mathrm{m}$, $h_2 = 150\,\mu\mathrm{m}$, $h_3 = 20\,\mu\mathrm{m}$ and $t = 20\,\mu\mathrm{m}$)

potential distribution is then used as an input for a quasi-magnetostatic simulation in order to calculate the current densities in the strip and in the semiconducting layer. From the current densities, the resistance and the inductance can easily be derived. The frequency range is extended down to 10 MHz, to get a better view of what happens at low frequencies.

The simulation geometry is similar to the geometry of the mode analysis simulation (Figure 3.14), however the width of the box is increased to 1 cm [3]. For the quasi-electrostatic simulation, the contour of the strip conductor is defined as a fixed input voltage V of 1 V amplitude. Originally, all the

[3]The quasi-static simulations are less computational intensive than the mode analysis, so the simulation geometry can be larger

outer boundaries were perfectly conducting with a reference potential of 0 V. However, due to the conductivity of the silicon, this forced the potential of the silicon domain to the reference potential, leading to inaccurate results for the shunt impedance parameters. To solve this, only the lower boundary is set at the reference potential and the remaining outer boundaries are non-conductive. The resulting potential distribution ϕ is transferred to the quasi-magnetostatic simulation, which calculates the perpendicular (or longitudinal) current densities. The total current is obtained by integrating the current densities over all the conductive domains, similar to equation (3.60).

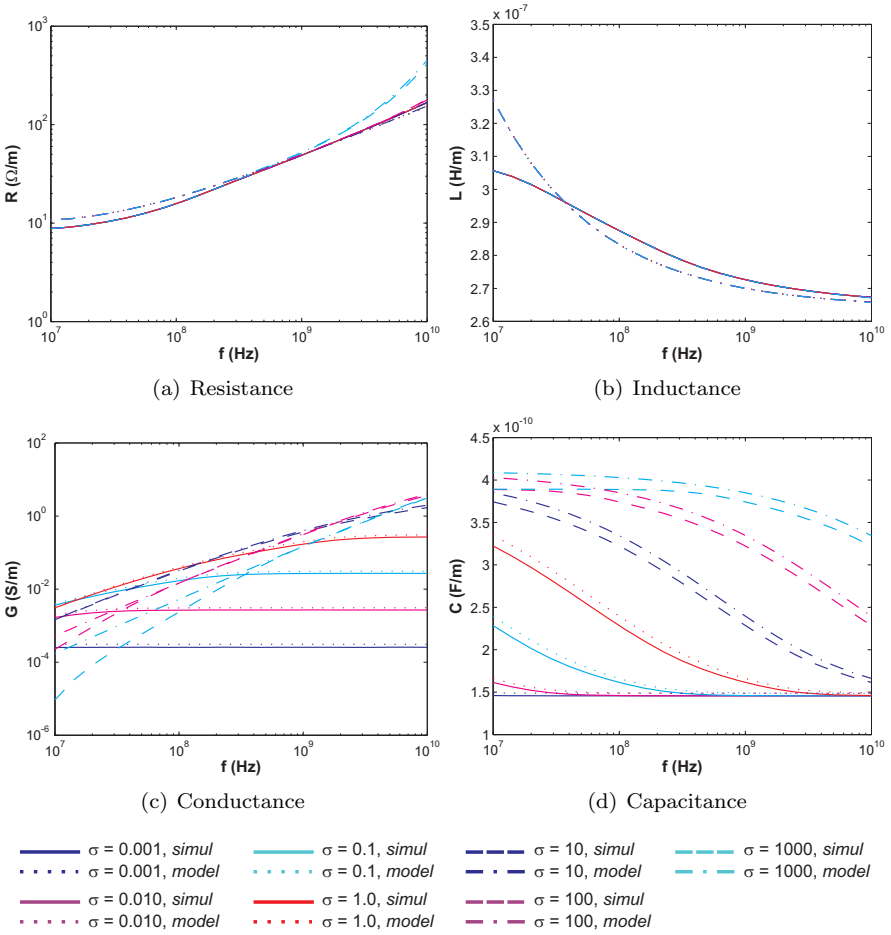
$$I = \int_{S_{Cu}} J_z \, \mathrm{d}S + \frac{1}{V^*} \int_{S_{Si}} J_z \phi^* \mathrm{d}S \tag{3.120}$$

The inductance and the resistance follow immediately from the total current and the potential of the strip.

$$R + j\omega L = \frac{V}{I} \tag{3.121}$$

Figure 3.18(a) to 3.18(d) respectively show the simulation results for the resistance, inductance, conductance and capacitance, compared to the values predicted by the model. Overall, the frequency-dependent behaviour predicted by the model is confirmed by the simulations. The influence of the silicon conductivity on the series impedance parameters for this geometry is negligible due to the very small height of the silicon layer. Only the resistance for the highest value of the conductivity ($\sigma_2 = 1000\,\mathrm{S/m}$) shows a small increase at high frequencies. Note that the incremental inductance rule, used for the resistance and the internal inductance, breaks down at low frequencies, where the skin depth is more than a third of the strip thickness (below 100 MHz for $t = 20\,\mu\mathrm{m}$). The shunt impedance parameters show the typical relaxation behaviour that was also apparent from the mode analysis simulations. The saturation of the simulated capacitance for high conductivities is strongly reduced. The influence of the finite width of the simulation geometry, as explained in equation (3.49), still results in a slight underestimation of the capacitance and conductance in the slow-wave region.

To better visualize the effect of the conductivity on the series impedance parameters, the results for a thicker silicon layer are shown in figure 3.19(a) to 3.19(d). The increase in resistance due to the longitudinal currents in the semiconducting layer is clearly visible on the graphs. The simulations and the model do not agree perfectly, but the introduction of the effective height gives a good representation of the effect. This is also the case for the inductance. The behaviour of the simulated conductance at high conductivities and below 100 MHz in figure 3.19(c) shows a large discrepancy with the model, which is again caused by the limited width of the simulation geometry. Overall, there



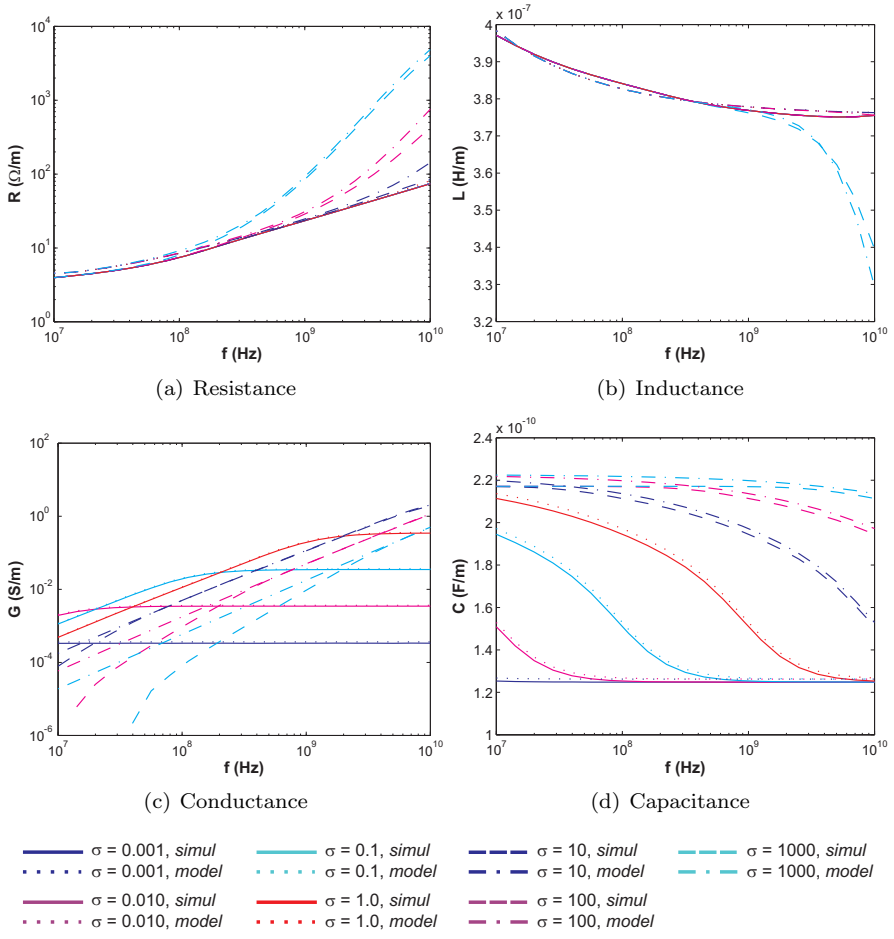
(a) Resistance (b) Inductance

(c) Conductance (d) Capacitance

Figure 3.18: Comparison between simulation results and the final model. All conductivity values in S/m ($w = 100\,\mu\text{m}$, $h_1 = 10\,\mu\text{m}$, $h_2 = 20\,\mu\text{m}$, $h_3 = 20\,\mu\text{m}$ and $t = 20\,\mu\text{m}$)

is a good correspondence between the simulation and the model, indicating that the single-layer reduction method and the effective height are two simple, but accurate methods for modelling the effect of semiconducting layers in a multilayer microstrip.

Detailed plots for the other geometries can be found in appendix D.



(a) Resistance (b) Inductance

(c) Conductance (d) Capacitance

Figure 3.19: Comparison between simulation results and the final model. All conductivity values in S/m ($w = 250\,\mu\text{m}$, $h_1 = 50\,\mu\text{m}$, $h_2 = 150\,\mu\text{m}$, $h_3 = 20\,\mu\text{m}$ and $t = 20\,\mu\text{m}$)

When comparing the different simulated geometries with the model, certain observations can be made on the accuracy of the model. However, to correctly judge the accuracy of the model versus the simulation, a reference benchmark

is required to determine the absolute accuracy of the different methods. An ultra-high precision benchmark for the validation of planar electromagnetic analyses has been proposed by Rautio in [76]. The characteristic impedance of an infinitely thin, perfect conducting stripline in air can be calculated analytically and is an excellent reference benchmark, since the accuracy is only limited by the numerical accuracy of the computer system. The simplicity of the geometry guarantees a universal application.

The single-layer reduction model and the finite-element method simulator were used to calculate the capacitance of the stripline geometry, using the width of the strip that corresponds to a $50\,\Omega$ impedance ($w = 1.4423896\,\text{mm}$ for 1 mm ground plane spacing according to [76]). The capacitance can be derived directly from the impedance ($C_0 = 1/(c\,Z_0)$) and the results are shown in table 3.2. The simulation in Comsol was performed twice: Once with a dense mesh and linear elements (20 902 degrees of freedom), which is similar to the settings used for the multilayer microstrip simulations, and a second time with the same mesh, but quintic elements to attain the highest possible accuracy (490 822 degrees of freedom). This increases the simulation time from 0.693 s to 26.188 s, and is impractical for more complex geometries.

As can be seen from table 3.2, the accuracy of the finite-element method simulation is very good, and near perfect when using the highest order elements. This indicates that attention to the mesh generation and the selection of the element order is important for the accuracy of the FEM simulation. As pointed out in the theoretical explanation, the capacitance calculated using the variational method is always smaller than the exact value. Here, it is about 2 % lower than the analytical solution, which is very good taking into account the symplicity of the model. While these results can not be extended to more complex geometries, they give a good indication of the inherit accuracy of both methods.

Table 3.2: Accuracy comparison for a reference stripline between the exact analytical solution, the single-layer reduction model and the Comsol FEM simulator. "L1" refers to the use of linear elements, "L5" refers to the use of quintic elements

	Analytical	SLR model	Comsol (L1)	Comsol (L5)
C_0 (pF)	66.66667	65.30314	67.02681	66.66152
rel. error	0.0	2.05e-2	0.54e-2	7.72e-5

The accuracy of the proposed model is expressed by the relative error between the final model and the multilayer microstrip simulations. Table 3.3 shows the average relative error for the different geometries. The average error is calculated across the entire frequency range and for the various silicon con-

ductivities. Between brackets, the peak relative error for that given geometry is displayed. Comparing these two values gives a good indication if there is an offset between the results or the difference is only located in a specific part of the frequency range.

Looking at the table, it is clear that there are quite some differences between the various parameters. The inductance shows an agreement to the simulations that is better than 2 % on average, and only slightly higher peak values. These are due to the fact that the incremental inductance rule breaks down at low frequencies. Again, it is clear that the effective height is an accurate way of moddeling the skin effect mode in a multilayer microstrip. For the capacitance, the overall error is slightly larger and there is a distinct correspondence between the average and the peak error, suggesting an almost constant offset between the model and the simulation. This is confirmed when looking at figures 3.18(d) and 3.19(d). Possible explanations are the finite width of the simulation geometry and the limited accuracy of the compensation that is used for the finite trace thickness (equation (3.74)).

For the loss of the microstrip, the relative error between the model and the simulation is two to three times larger. A number of discrepancies were already identified before, namely the poor accuracy of the incremental inductance rule for the resistance at low frequencies and the erroneous behaviour of the conductance for high silicon conductivities. To get a correct view of the *overall* accuracy of the model, these known issues are not included in the calculation of the relative error. In practice, the frequency range for the average error of the resistance is limited to 100 MHz to 10 GHz and the highest conductivities ($\sigma > 10\,\mathrm{S/m}$) are excluded from the conductance error calculation. Despite this, the relative error for the resistance and the conductance are still quite large. Since the conductance is based on the same calculation of the effective dielectric constant as the capacitance, a similar offset between the simulation and the model is present. In addition, the high range of values for the conductance, from very low to very high, can cause small absolute errors to have a high impact and vice versa. For example, the relative error is the highest for the geometries with low conductance values ($w = 100\,\mu\mathrm{m}$ and $h_2 = 20\,\mu\mathrm{m}$). On the other hand, the average error of the resistance is larger for wide strips ($w = 250\,\mu\mathrm{m}$) and thicker silicon ($h_2 = 20\,\mu\mathrm{m}$). The formula for the conductive loss in the copper trace fails to accurately describe the current distribution for wide strips at high frequencies. For thick silicon, the approximations made for the effective height mimic the behaviour of the current crowding in the semiconducting layer quite well but do not achieve the highest numerical accuracy.

These relative errors are an indication of the accuracy of the model. However, since the absolute error of the simulations itself can not be determined, these numbers do not tell the complete story. The real error analysis has to be performed using real-life measurements.

Table 3.3: Calculated average relative error (*peak rel. error*) for the final model versus the simulations ($h_3 = 20\,\mu m$, $t = 20\,\mu m$)

w	h_1	h_2	$\Delta R/R$	$\Delta L/L$	$\Delta G/G$	$\Delta C/C$
100	10	20	0.05 (*0.13*)	0.014 (*0.016*)	0.17 (*0.17*)	0.038 (*0.047*)
250	10	20	0.06 (*0.12*)	0.015 (*0.017*)	0.11 (*0.12*)	0.039 (*0.050*)
100	10	150	0.15 (*0.46*)	0.007 (*0.018*)	0.09 (*0.09*)	0.029 (*0.040*)
250	10	150	0.17 (*0.51*)	0.005 (*0.025*)	0.09 (*0.09*)	0.030 (*0.040*)
100	50	20	0.06 (*0.21*)	0.012 (*0.019*)	0.24 (*0.24*)	0.003 (*0.006*)
250	50	20	0.11 (*0.32*)	0.017 (*0.023*)	0.10 (*0.10*)	0.026 (*0.027*)
100	50	150	0.13 (*0.31*)	0.006 (*0.012*)	0.05 (*0.06*)	0.060 (*0.063*)
250	50	150	0.16 (*0.44*)	0.004 (*0.031*)	0.08 (*0.08*)	0.012 (*0.014*)

3.3 Conclusion

The characterization of tracks running on top of embedded components can be reduced to modelling the mixture of conductive and non-conductive layers in the substrate of a microstrip transmission line. The physical behaviour of these multilayer substrates can be explained using the parallel-plate approximation. Three different propagation modes can be distinguished, depending on the frequency and the conductivity of the semiconducting layer. At high frequencies combined with low conductivity, the semiconducting layer acts as a dielectric and can be modelled similar to the non-conductive layers. When the conductivity is higher, the fields will fail to penetrate the silicon layer due to the skin effect. At intermediate frequencies, the high conductivity will give rise to an increased effective dielectric constant and thus a slower propagation velocity. These three regions are respectively referred to as the dielectric mode, skin effect mode and slow-wave mode and result in a strong frequency dependence of the per-unit-length parameters.

The parallel-plate approximation fails to accurately predict the propagation constant of the slow-wave mode and is replaced by the multilayer microstrip model. This model is based on two similar techniques that reduce the multilayer substrate into an equivalent single-layer substrate. In a first step, the slow-wave behaviour is modelled using the single-layer reduction technique, that uses a variational expression to calculate the complex line capacitance. To incorporate the effect of the current crowding in the silicon layer, the concept of the effective height is introduced using the complex image approach. The two simplifications lead to a fast and flexible model with sufficient accuracy, that can be used in design rules and formulas similar to those available for standard microstrip transmission lines.

To verify the practicality of the model and to draw the final verdict on

its accuracy, a verification using measurements is required. An accurate and simple technique to extract the propagation parameters from the measurements is introduced in the next chapter.

Chapter 4

Methodology for parameter extraction

In a recent survey on dwarfs 6 out of 7 weren't Happy.

4.1 Introduction

The extraction of material and transmission line parameters is crucial for the validation of modelling and simulation results. In this chapter, a powerful and versatile methodology for parameter extraction based on the multiline TRL (ML-TRL) calibration technique is revealed. Section 4.2 describes the propagation constant extraction based on the multiline TRL calibration, while section 4.3 goes into details about the determination of the dielectric constant and the loss factor, specifically for geometries found in printed circuit board applications. The methodology is applied to the extraction of material parameters for modern laminate materials to illustrate the accuracy and flexibility of this technique.

4.2 Propagation constant extraction

Regardless of the final goal of the characterisation, whether it is material parameter evaluation or modelling of embedded chips, there is a need for a highly accurate parameter extraction method which is both simple to implement and powerful. High accuracy requires the removal of all external and parasitic influences, as well as probe and contact pad disturbance. Probe tip calibration and measurement structure de-embedding are good solutions, but often require

lots of extra test structures as well as dedicated parasitic modelling. The proposed method offers both simplicity and flexibility, while offering calibration level accuracy.

The method is based on the extraction of the propagation constant as part of the multiline Thru-Reflect-Line (TRL) calibration [77]. This calibration technique was developed to overcome the bandwidth limitations of the high accuracy TRL calibration and was initially introduced as an on-wafer calibration. The calibration structures consist of a thru, a reflect and at least two additional lines of different length, and thus require very little space. Where the standard TRL calibration relies on a single line for each part of the frequency span, the multiline TRL approach optimises the results from different line pairs over the complete frequency range.

As with the conventional TRL calibration, the aim is to calculate the error boxes, which are usually described by the cascade-parameters:

$$M_i = XT_i\bar{Y} \tag{4.1}$$

where

$$\bar{Y} = \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix} Y^{-1} \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix} \tag{4.2}$$

With M_i being the measured cascade parameters for line i, T_i the cascade parameters of the line standard and X and Y the error box parameters. The cascade parameters can be easily derived from the measured S-parameters. Prior to performing the measurement, the network analyser is calibrated up to the probe tips using a commercial calibration substrate. As a result, the error boxes of the second tier calibration in this case only contain the influence of the probe contacts and the impedance transformation from the measurement system (typically $50\,\Omega$) to the characteristic impedance of the line standards. The difference for the multiline calibration compared to the classic TRL implementation is the combination of line pairs with different lengths to reduce the number of unknown parameters. Inverting (4.1) for line i and multiplying by M_j leads to the following equation.

$$M_j \left(M_i\right)^{-1} = XT_j\bar{Y} \left(\bar{Y}\right)^{-1} \left(T_i\right)^{-1} \left(X\right)^{-1} \tag{4.3}$$

or

$$M_{ij}X = XT_{ij} \tag{4.4}$$

where

$$M_{ij} = M_j \left(M_i\right)^{-1} \tag{4.5}$$

$$T_{ij} = T_j \left(T_i\right)^{-1} \tag{4.6}$$

Since the impedance transformation is incorporated in the error box, a matched transmission line model can be used as ideal line standard.

$$T_i = \begin{bmatrix} e^{-\gamma l_i} & 0 \\ 0 & e^{+\gamma l_i} \end{bmatrix} \tag{4.7}$$

Resulting in

$$T_{ij} = \begin{bmatrix} e^{-\gamma (l_j - l_i)} & 0 \\ 0 & e^{+\gamma (l_j - l_i)} \end{bmatrix} \tag{4.8}$$

Introducing this into (4.4), leads to an eigenvalue problem, where the diagonal elements of the matrix T_{ij} are the eigenvalues of M_{ij} and the columns of X are the eigenvectors of M_{ij}. Since the line differences are known, the propagation constant can be easily calculated from the eigenvalues for each line pair. The propagation constant extraction, along with the calculation of the error boxes, has been implemented in MATLAB. The description of the algorithm can be found in appendix E. A detailed analysis of the calibration algorithm, as can be found in [77], shows that even for non-ideal line standards, the diagonal elements of T_{ij} in (4.4) are still determined by the eigenvalues of M_{ij}.

The interesting part about this approach is that the error boxes include all the parasitic effects of the probe contacts, but do not need to be known to extract the propagation constant. The second advantage is that the line pairs in this method can be implemented as any kind of transmission line, being microstrip, stripline or coaxial cable. Errors due to uncertainties of the length, for example by under etching or probe placement, are correlated for all line standards, and are eliminated in the algorithm since only the difference in length is used. The multiline TRL calibration thereby offers an accurate propagation constant extraction for a wide range of implementations. The idea of extracting the permittivity from the propagation constant obtained through the multiline TRL calibration has been suggested in [78]; however the tested technique required a sample to be inserted in a waveguide or coaxial transmission line. The strength of the method here is that the calibration structures can be implemented on the final layout and build-up of the printed circuit board.

The minimum set to extract the propagation constant consists of a thru standard, which basically is a very short line, and another line standard of different length, preferably as long as possible. For this minimum set the method becomes inaccurate at frequencies where the phase difference between the two lines is close to a multiple of 180 degrees (0°, 180°, 360° ...). By maximizing the line difference, the frequency ranges where these anomalies occur are minimized in width. To circumvent this problem, e.g. when long lines are not available, the multiline TRL calibration adds an extra line structure to extract the propagation constant at these frequencies, increasing the overall accuracy. The risk of inhomogeneous areas, as for example fibre bundles, distorting the

result is also reduced by using additional lines. Unlike for the classic TRL calibration, there is no straightforward calculation for the ideal length of the test structures. Using a line length of a quarter wavelength at the centre frequency, and another one of three times that length was suggested by Marks [77], but the author admits that this is certainly not a limit for the validity of the calibration. Calculation of the effective phase difference, also described in [77], can give an indication of the calibration accuracy across the targeted frequency range as the error is proportional to $1 \,/\, |\sin(\Phi_{eff})|$.

$$\Phi_{eff} = \arcsin\left(\frac{1}{2}\left[\exp\left(-j\frac{\omega}{c}\sqrt{\epsilon_{eff}}\Delta l\right) - \exp\left(j\frac{\omega}{c}\sqrt{\epsilon_{eff}}\Delta l\right)\right]\right) \tag{4.9}$$

4.3 Material parameter extraction

One of the big advantages of the propagation extraction method based on the multiline TRL calibration is that there is no specific model used for the calibration standards, which are only assumed to be transmission lines. This allows for the calibration method to be implemented on a wide range of substrates, ranging from wafers to printed circuit boards. There is also no need for numerical approximations or empirical formulae in the calibration algorithm, so these cannot affect the accuracy. For this research simple microstrip test structures were used, since they are, along with striplines, the most common RF structures used in printed circuit boards. Another advantage is the possibility to study the parasitic high-frequency behaviour of copper tracks even if these traces are not intended for high-frequency applications. As described in section 4.4.2, PCB processing has several compromises between manufacturability and high-frequency behaviour. In order to extract the correct material parameters (ϵ_r,$\tan\delta$) from the propagation constant γ, all these aspects need to be incorporated in the model.

The propagation constant can be split up into a loss factor α and the phase shift β. Losses for microstrips are dominated by skin effect and dielectric loss, with the latter becoming more significant at high frequencies. The phase shift can be related directly to the effective dielectric constant; however a compensation for the decrease in inductance caused by the skin effect is needed to obtain the correct value at low frequencies [79].

To extract the material parameters from the propagation constant, the per-unit-length $RLGC$ parameters are calculated as an intermediate step.

$$\gamma = \alpha + j\beta = \sqrt{R + j\omega L}\sqrt{G + j\omega C} \tag{4.10}$$

$$Z = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \tag{4.11}$$

These expression can be simplified using the Taylor series of $\sqrt{1+x}$ for $|x| \ll 1$. Assuming $R \ll \omega L$ and $G \ll \omega C$, the following approximations can be made.

$$\begin{aligned}\gamma &= j\omega\sqrt{LC}\sqrt{1+\frac{RC+GL}{j\omega LC}} \approx j\omega\sqrt{LC}\left(1+\frac{1}{2}\frac{RC+GL}{j\omega LC}\right)\\ &\approx \frac{1}{2}\left(\frac{R}{\Re(Z_0)}+G\,\Re(Z_0)\right)+j\omega\sqrt{LC} \qquad (4.12)\\ Z &= \sqrt{\frac{L}{C}}\sqrt{\frac{1+\dfrac{R}{j\omega L}}{1+\dfrac{G}{j\omega C}}} \approx \sqrt{\frac{L}{C}}\frac{1+\dfrac{R}{2j\omega L}}{1+\dfrac{G}{2j\omega C}}\\ &\approx \sqrt{\frac{L}{C}}\left(1+j\left(\frac{G}{2\omega C}-\frac{R}{2\omega L}\right)\right) \qquad (4.13)\end{aligned}$$

Resistive loss can be easily and accurately calculated from the conductivity of the copper and the geometry of the microstrip. The DC resistance per-unit-length can be calculated in a straightforward manner from the conductivity of the copper (σ) and the area of the cross-section of the signal conductor. The frequency dependence of the AC resistance is determined by the skin effect, assuming the current flows in a thin layer with thickness δ_{Cu} at the circumference of the signal conductor ($t \gg \delta_{Cu}$) [1]. By using a proximity factor k_p of 2, it is assumed that at high frequencies all the current in the ground plane is located underneath the microstrip trace. To incorporate the effect of the surface roughness, an empirical roughness-factor k_r is added to the formula for R_{AC}, raising the resistance by a factor of 2 at high frequencies [32]. The transition frequency for this increase in resistance is dependent on the RMS-value of the roughness, which can be measured directly on the copper foil or estimated from cross-sections, and can range from less than 0.5 µm to several micrometer. The value used in this research was determined based on information found in the material data sheets and is of the order of 1 µm. This leads to the following

[1] This is a common approximation for the AC resistance. However, for a rectangular shaped microstrip trace, the absolute error is $4\delta_{Cu}$. This error is maximal for $t = 2\delta_{Cu}$ and corresponds to a relative error of t/w. Thus, the accuracy of this approximation brakes down quickly at lower frequencies (below 1 GHz).

formulae [32]:

$$\alpha_c = \frac{1}{2}\frac{R_{DC} + R_{AC}}{\Re(Z_0)} \tag{4.14}$$

$$R_{DC} = \frac{1}{w\sigma t} \tag{4.15}$$

$$R_{AC} = \frac{k_r k_p}{2\,(w+t)}\sqrt{\frac{\pi f \mu}{\sigma}} = \frac{k_r}{w+t}\sqrt{\frac{\pi f \mu}{\sigma}} \tag{4.16}$$

$$k_r = 1 + \frac{2}{\pi}\arctan(1.4\pi f \mu \sigma h_{RMS}^2) \tag{4.17}$$

At higher frequencies the dielectric loss becomes dominant over the conductive loss. In order to determine the material parameters, the dielectric loss can be expressed as a function of the loss factor $\tan\delta$ [32].

$$\alpha_d = \frac{1}{2} G\,\Re(Z_0) = \frac{1}{2}\omega\frac{\sqrt{\epsilon_{eff}}}{c}\tan\delta \tag{4.18}$$

The effective value of the dielectric constant can be extracted from the imaginary part of the propagation constant, the phase shift β. Before extracting the effective value of the dielectric constant from the phase shift β, a correction for the increase in internal inductance at low frequencies has to be applied. This correction was derived by relating the per-unit-length parameters to the propagation constant, with and without the effect of the internal inductance.

$$\begin{aligned}\beta &= \omega\sqrt{(L_{ext} + L_{int})\,C} \approx \omega\sqrt{L_{ext}C}\left(1 + \frac{1}{2}\frac{L_{int}}{L_{ext}}\right) \\ &\approx \omega\frac{\sqrt{\epsilon_{eff}}}{c} + \frac{1}{2}\frac{R_{AC}}{\Re(Z_0)}\end{aligned} \tag{4.19}$$

The difficulty is that this formula requires the knowledge of the (real part of the) characteristic impedance of the transmission line structures; but fortunately the correction is not very sensitive to the accuracy of the characteristic impedance. Since the propagation constant is known already, the characteristic impedance can be calculated by determining the capacitance of the microstrip (assuming low dielectric loss).

$$\Re(Z_0) = \frac{\beta}{\omega C_0} \tag{4.20}$$

The capacitance can be calculated using the empirical formula from section 4.4.2, requiring the knowledge of the effective dielectric constant of the microstrip. The solution to this circular dependency is to extract the effective dielectric constant without the skin effect correction and use this to calculate

the capacitance of the microstrip structure. After calculating the characteristic impedance from the capacitance, the correction can be applied to the phase shift. The last step can be iterated several times, each time adjusting the correction to the phase shift to increase accuracy, but due to the limited influence on the accuracy more than 1 or 2 times is not required.

4.4 Application to modern PCB materials

4.4.1 Introduction

Modern applications, ranging from high-speed telecommunication systems to automotive industries, impose new requirements on printed circuit board laminates. New materials are being developed to compensate the drawbacks of classic FR4 materials, such as low glass transition temperature (T_g), high thermal expansion (CTE) and high dielectric constant (ϵ_r). There is a strong need to characterize the high-frequency behaviour of these new materials, taking into account the limitations of current printed circuit board processing.

Mainstream acceptance of several new technologies, such as high-definition video processing and high-performance computing introduces high-bandwidth applications in high-volume production. Due to cost limitations special high-frequency techniques and materials can not be used here, and the limits of traditional printed circuit board processing with regard to high-frequency behaviour become visible: high track thickness, solder mask, surface finish, and presence of glass fibres (Fig. 4.1). Even when the final implementation justifies the use of special materials, compromises need to be made, sacrificing performance for cost and manufacturability.

These compromises can have a great influence on the high-frequency behaviour of the system and therefore there is a strong need to quantify these issues. The method presented in the previous sections was developed for broadband material characterization by extracting the material parameters as dielectric constant and loss tangent. The high accuracy and real-world implementation of this technique make it possible to investigate the effect of different processing techniques and design trade-offs over a wide frequency range.

4.4.2 Problem description

Numerous techniques for extracting the dielectric constant and loss tangent have been developed in the past. These techniques were targeted at a wide range of frequencies and a variety of different implementations, ranging from Monolithic Microwave Integrated Circuits, over cable dielectrics, to printed circuit board applications. Each solution requires dedicated test apparatus or

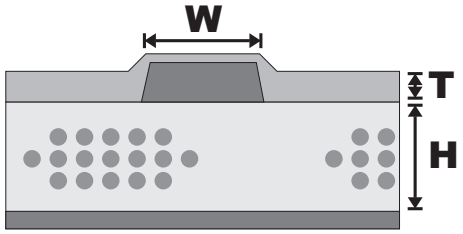


Figure 4.1: Microstrip geometry with glass fibres, solder mask and high track thickness

test structures, making it difficult to compare the accuracy of the extracted parameters. In the case of printed circuit board materials characterization was typically performed at low frequencies (1 MHz), based on capacitance measurements of the bare material (IPC-TM-650 method 2.5.5). These methods require the removal of the copper and can only be used to test the bare material outside of its typical implementation. More recent techniques use open-ended coaxial lines or waveguides [80], transmission/reflection measurements [81], resonant frequencies of dedicated resonator structures or cavities [82, 83], time-domain measurements [84], or transmission line parameter matching to determine the material parameters at different frequency points. The methods from this last category, such as the one presented in the previous section, can be used in a large field of application and over a wide frequency range and can be implemented in a manner close to the real-world use of the materials.

Material data sheets supplied by the manufacturer are now increasingly using these new techniques to present the material parameters at higher frequencies (> 1 GHz) and sometimes even at multiple frequency points. Frequency-dependent data over a wide frequency range are still not common in material data sheets, while for example high T_g, low CTE printed circuit board materials seem to show a stronger dependency on frequency than FR4.

Design rules and formulae for planar transmission lines such as microstrips and striplines were developed based on empirical data and electromagnetic simulations. Most of these formulae use the classical geometry found on integrated circuits, meaning thin strips on top of a monolithic substrate. Frequency ranges that were typical for on-chip applications are now found on board interconnect. However the manufacturing process for these printed circuit boards is totally different from the fine line processing in silicon technology, with much higher tolerances.

The first compromise has to be made based on the mechanical stability of the substrate. Thermal expansion in X- and Y-direction is minimized by the use of glass fibre weaves in combination with a polymer resin. Due to higher reflow temperatures in lead-free processing, materials with a high glass

transition temperature (T_g) and low constant of thermal expansion (CTE) in the Z-direction were needed to increase reliability. These materials were realized by using special resins, but also by adding ceramic fillers to the polymer mixture. Glass fibres and ceramic fillers raise the dielectric constant of the composite material and fibre bundles also introduce a space-dependency for the dielectric constant [32]. Decreasing line widths of the copper tracks and lower thickness of the base materials are making the effect of the glass fibres on high-frequency behaviour more and more apparent. Environmental concerns on flame-retardants also impose new limitations on the chemical content of printed circuit board materials. Material data sheet nowadays often list a range of values for the dielectric constant, sometimes even based on resin content, but a more detailed study of the frequency-dependent behaviour is required to allow for an improved high-frequency design.

Higher reflow temperatures result in additional stress at the interfaces between copper and dielectric materials. In order to prevent delamination, an adhesion promotion step is required. This is traditionally performed by adding some roughness to the copper surface to enlarge the contact area. This roughness manifests itself as so called dendrites, long finger-like structures of several micrometers long. At low frequencies the depth of penetration of the current exceeds the root-mean-square height of these structures, so their influence remains small. High-frequency currents flow close to the surface, following the contour of that surface and resulting in an increase in resistance because of the additional distance the currents must flow. The development of, e.g., Profile-Free Copper by Hitachi Chemicals [85], combining low roughness with good adhesion, shows that this issue is taken seriously by material manufacturers.

After vacuum lamination of the inner and outer layers of the printed circuit board, the boards are moved to the drilling process. This can be either mechanical drilling for through-holes or laser drilling for the microvias. The electrical contact between the layers is achieved by depositing copper on the walls of the vias by galvanic copper plating. To assure good reliability a copper thickness of 15 µm to 25 µm inside the via is required. Depending on the thickness of the base copper on top, this results in a track thickness of 30 µm to 50 µm. Non-uniformity of copper plating and etching across the board can also cause impedance variations for long tracks. In combination with the decreasing dielectric height for the outer layers, the ratio of the track thickness to the height of the dielectric is changing from 0.1 to 0.5, and even close to 1 in some cases. Classic formulae were only developed and tested for $t/h < 0.2$ [75] and little research has been done to the validity of these formulae beyond this range[2].

[2]An alternative to these closed form expressions is to use 2D planar EM solvers, which provide accurate results for a wide range of geometries. These solvers excel in the analysis and synthesis of individual transmission lines, but still require a lot of computational resources to simulate complex circuits with multiple distributed components.

To get a quantitative idea of the influence of the track thickness, the capacitance of a microstrip was simulated for different copper thickness. The capacitance of a microstrip is directly related to its characteristic impedance and can be easily extracted using electromagnetic simulations. Fig. 4.2 shows the results of the simulation. When the thickness of the copper increases from 10 µm to 50 µm, there is a raise in capacitance of up to 20 %, resulting in a similar decrease in characteristic impedance. If the ratio of the thickness to the width of the strip is low, the track thickness has a smaller influence on the capacitance. For a higher circuit density, a smaller line width is needed. This results in a decrease in substrate height to maintain the same controlled impedance. Therefore the influence of track thickness is becoming more and more important. Formulae as those developed by Schneider [86] and Wheeler [60], can accurately predict the capacitance of a microstrip with finite track thickness, but the error increases when the thickness becomes equal to the substrate height and the width of the microstrip.

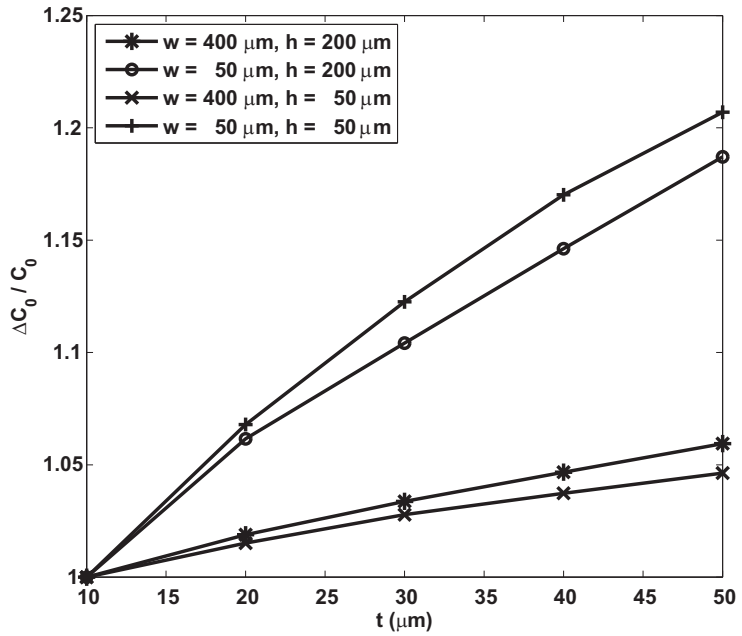


Figure 4.2: Relative increase in capacitance as a result of increasing microstrip trace thickness t for different combinations of substrate height h and strip width w

One of the final steps in the printed circuit board manufacturing process is the application of the surface finish and the solder mask. Both of them have a strong influence on the high-frequency behaviour of the microstrip. When

a solder mask is applied, the surface finish will be limited to the open pads, and thus the effect on the high-frequency behaviour of the surface finish will be minimized. The presence of the solder mask will however have a great influence on the effective dielectric constant of the microstrip. Practical solder mask materials have a high dielectric constant compared to modern high-frequency laminates. The solder mask covers the copper trace with a coating of 10 µm to 20 µm, effectively surrounding part of the microstrip with an additional dielectric layer. Skipping the solder mask in critical areas is not recommended because then the surface finish is applied to the entire copper pattern on the outer layers. In the case of Ni/Au, with nickel being slightly magnetic and less conductive than copper, the negative effect on the performance is far greater, raising the conductive loss at high frequencies and lowering the propagation velocity [87].

In order to investigate the effect of a high track thickness with the presence of a solder mask, a second series of electrostatic finite element simulations was performed. A microstrip structure with solder mask (Figure 4.1) was simulated twice, once to calculate the capacitance without any dielectric, and once to calculate the capacitance with a dielectric substrate ($\epsilon_r = 3$, 4 or 5) and solder mask ($\epsilon_r = 4.2$). The ratio of these two capacitance values is the effective dielectric constant of the microstrip structure. A number of different dimensions were simulated, with the height of the substrate ranging from 50 µm to 100 µm, the width of the strips from 70 µm to 120 µm and the thickness from 20 µm to 50 µm. The solder mask extends 10 µm above the trace and the thickness next to the microstrip is equal to the trace thickness. These dimensions reflect those of the measurement test structures (see section 4.4.3). Figure 4.3 displays the results for a substrate with a relative dielectric constant of 3. The lower group shows the results without solder mask. The discrete results for each value of w/h are due to the variation of the thickness of the microstrip, depending on the ratio of the thickness to the height and the width of the microstrip. The effective dielectric constant decreases with increasing thickness of the copper. The upper cluster of simulation results in Fig. 4.3 take into account the presence of the solder mask ($\epsilon_r = 4.2$), and reveal a difference of up to 40 %. This justifies the adaptation to the conversion formula from effective to relative dielectric constant in the presence of a solder mask.

A correction term for the solder mask with dielectric constant ϵ_{SM} was added to the conversion formula for the effective dielectric constant [75]. The coefficients of these formulae were then fitted to the simulations of the microstrips with high track thickness and solder mask. This formula yields satisfying results for the dimensions used in this project. More extensive simulations and parameter fitting are required to validate the formula for other geometries.

$$\epsilon_{eff} = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2} F - C + SM \tag{4.21}$$

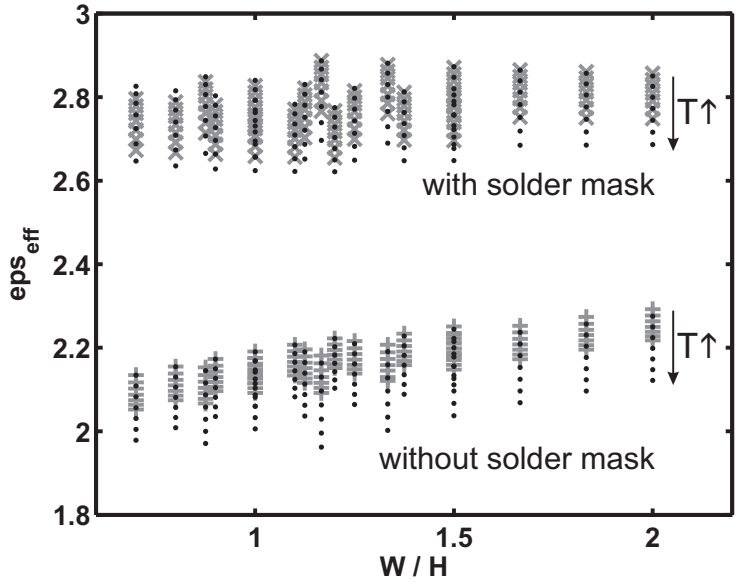


Figure 4.3: Simulation results for the effective dielectric constant (dots) versus the width to height ratio of a microstrip with and without solder mask and for varying strip thickness. The grey markers indicate the calculated value using the conversion formula of Schneider (lower group, +) and the adapted formula (upper group, ×)

$$F = \begin{cases} \frac{1}{1.71}(1+12\frac{h}{w})^{-\frac{1}{2}} + 0.04(1-\frac{w}{h})^2 & (\frac{w}{h} \leq 1) \\ \frac{1}{1.71}(1+12\frac{h}{w})^{-\frac{1}{2}} & (\frac{w}{h} \geq 1) \end{cases} \tag{4.22}$$

$$C = \frac{\epsilon_r - 1}{7.9}\frac{t}{h}\sqrt{\frac{h}{w}} \tag{4.23}$$

$$SM = 0.11(\epsilon_{SM} - 1)(1.5 - (\frac{t}{w} - 1)^2)\sqrt{0.6\epsilon_r + \frac{t}{h}} \tag{4.24}$$

The effective value of the loss factor $\tan\delta$ can be calculated based on ϵ_{eff}.

$$\tan\delta_{eff} = \tan\delta\frac{\epsilon_{eff} - 1}{\epsilon_{eff}}\frac{\epsilon_r}{\epsilon_r - 1} \tag{4.25}$$

The increasing track thickness and the problem of solder mask and surface finish are only related to microstrips. A solution could be the use of striplines, which are applied often in high data rate applications like backplanes

for routers. This requires extra layers and the signal via to the stripline can also cause problems at high frequencies. Looking at differential lines, microstrip pairs have a tighter pitch, a lower total dielectric thickness and a reduced dielectric attenuation due to the lower effective dielectric constant. For cost-effective solutions where space is limited, as for example mobile applications, or when dedicated RF design is not possible, microstrips are still used for transporting high-frequency signals.

For wideband and digital applications, a characterization of the material parameters across the entire frequency range is required. The characterization is not only needed for the substrate material, but also for the solder mask, the surface finish, plating thickness and glass fibre weave. By quantifying the relative influence of these materials and processing steps, the necessary compromises and possible design adaptations can be made.

4.4.3 Results and discussion

In the frame of the EMCOMIT project (IWT-PIDEA), a dedicated test vehicle was designed to investigate the material properties of laminate materials for printed circuit board manufacturing. A selection of materials with different application areas was used to produce these test boards. The test structures for this study consisted of a 2.5 mm long thru, a 12.5 mm line and a 32.5 mm line (Figure 4.4). The test boards also contained lines of 27.5 mm, 62.5 mm and 97.5 mm as a reference. The microstrip test structures were implemented four times for each material, two times on the top layer and two times on the bottom layer of the 8 layer test board.

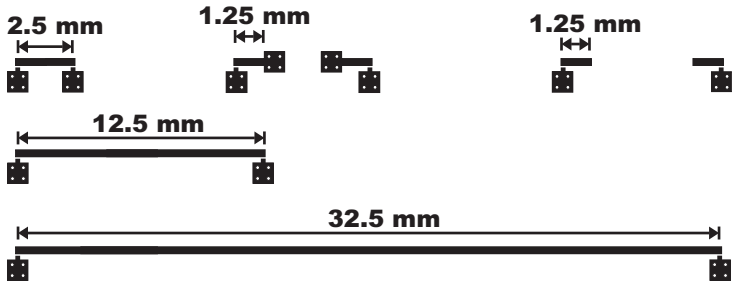


Figure 4.4: Test structures for the multiline TRL calibration (left to right and top to bottom: Thru, Reflect (short), Reflect (open), Line 1 and Line 2)

The measurements were performed using an Agilent PNA 8364B vector network analyser in a frequency range from 100 MHz up to 20 GHz. The test structures were contacted using coplanar microwave probes (Picoprobe 50A-GS/SG-500-P) and a dedicated printed circuit board probe table. A planar

Table 4.1: Comparison of the measurement results to the specifications supplied by the manufacturers

Material	ϵ_r	$\tan\delta$	ϵ_r	$\tan\delta$	Properties
	Spec(1 GHz)		Meas(1 GHz)		
PCL-370	4.3	0.015	4.1	0.020	FR4, high T_g
LX-67Y	3.5	0.004	3.6	0.010	High-frequency
MCL-E-679FJ	4.4	0.019	4.4	0.023	High T_g, low CTE
MCL-E-679FG	4.7	0.019	4.6	0.022	Halogen free
IS-420	5.1	0.015	4.7	0.025	High T_g, low CTE

LRM calibration was performed to compensate for internal errors of the network analyser and the cables, shifting the reference plane to the probe tips.

To compare the high-frequency behaviour of advanced laminate materials, a reference material is needed that is used in standard printed circuit board processing. The most wide spread base material is still FR4. In this study, the Polyclad PCL-370 was used, which is a FR4 material with a high glass transition temperature, offering improved thermal, mechanical and electrical performance compared to classic FR4. Materials for high-frequency applications use special compounds with low dielectric constant and low dielectric loss. Since the cost of these materials is usually a lot higher than the standard FR4, the advantages in high-frequency behaviour have to be large in order to convince the designer. The Hitachi material LX-67Y lives up to these expectations, with a reasonably low dielectric constant, but far less dielectric loss compared to standard FR4. High reflow temperatures for lead-free soldering and extreme conditions in, for example, automotive applications impose new requirements for the thermal expansion of printed circuit board materials. Low CTE in the z-direction is achieved by adding special filler-materials, which often cause deterioration in high-frequency performance. Replacements for halogen flame-retardants show a similar influence. These materials are not targeted towards high-frequency applications; however even low frequency digital signals can have a frequency content extending into the GHz range. Three such materials were investigated: Hitachi MCL-E-679FJ, Hitachi MCL-E-679FG (halogen free) and Isola IS-420.

While processing the measurement data, it became clear that the extraction of the propagation constant using the multiline TRL calibration is a very powerful technique. The results not only reveal the expected differences between the materials, but clearly show the influence of resin content, the presence of fibre bundles and differences in geometry for the different test structures for each material.

Table 4.1 shows the measurement results in comparison with the specifica-

tions supplied by the manufacturers. Overall there is a very good agreement between the data sheet specifications and the measured values, although these values are often at the lower boundaries of the specifications. This can be explained by the use of very thin prepreg materials (65 µm to 80 µm), which have a higher resin content (56 % to 71 %), resulting in a lower dielectric constant and higher dielectric loss. Looking at the Isola material, the data sheet specifies a maximum dielectric constant of 5.1, referring to laminates with the lowest resin content (41 %). A simple volume-percent calculation, using a dielectric constant of 6 for the glass fibres and a resin content of 62 % for the prepregs used for the test boards, reveals a theoretic dielectric constant of 4.67. This is in better agreement with the measurements.

The values for the dielectric constant have been corrected for the presence of a solder mask, however this is not the case for the dielectric loss, because it is not straight-forward to distinguish between the loss of the material and that of the solder mask. Neither was there any consistent data available for the loss factor of the solder mask. Judging from the differences for the dielectric constant, we can assume that, especially for the low loss materials the difference can be up to 20 %. Since in practical applications these materials are often used in combination with a solder mask, the results presented here for microstrips can still be useful for designers and material manufacturers.

Looking at the frequency-dependent behaviour of the materials (Figure 4.5 and 4.6), a typical behaviour of slowly declining dielectric constant for printed circuit board materials is revealed. The frequency dependence is stronger at lower frequencies, taking into account that due to the limited length of the microstrip lines, the results are less accurate at frequencies below 500 MHz. The low CTE materials not only have a higher value for the dielectric constant and loss tangent, but also show a stronger dependence on frequency compared to the standard FR4. On the other hand, the value for the dielectric constant of the high-frequency material shows less variation across the frequency spectrum. The loss factor for this material is higher than expected, which is likely due to the presence of the solder mask. This underlines the claim that surface coating plays an important role when choosing a high-frequency material for low loss applications.

Since the loss factor is calculated by subtracting the conductive loss from the measured attenuation constant, secondary loss mechanisms as radiation loss and non-linear effects are still present in the measurement results. The resonance peaks in the loss factor occur at the same frequencies for all the materials, which suggests that these are related to the initial planar LRM calibration.

Due to the low value of the dielectric constant of the high-frequency material, the influence of the glass fibre weave is more distinct. Figure 4.7 shows the effective dielectric constant for the test structures on the high-frequency

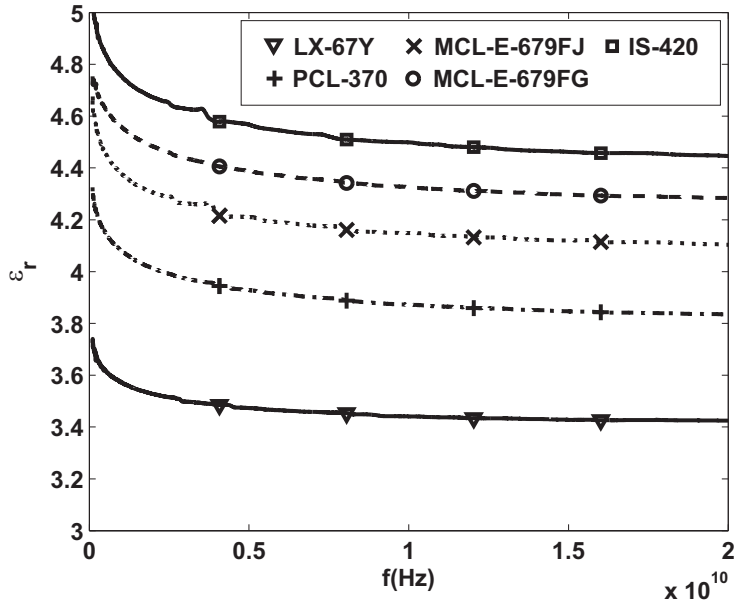


Figure 4.5: Frequency-dependent behaviour of the relative dielectric constant for the different printed circuit board materials

material test board at different locations on the board. These effective values were extracted directly from the propagation constant, only corrected for the skin effect. Microstrip trace A is located right on top of a fibre bundle, revealing a much higher value compared to trace B falling in between two fibre bundles (Figure 4.8). Because of the low value of the dielectric constant of the compound in between the fibres, combined with the high resin content of the material, there is quite a large difference between the minimum and maximum value. Relating these values to Figure 4.5, it is possible that a material with a lower average ϵ_r has a higher effective dielectric constant for certain traces. The average values should still be used for design purposes, since it is not possible to know in advance what the location of the trace is going to be in respect to the fibre bundle below. If the difference in propagation time is critical, alternative solutions as angled routing or special fibre weaves need to be taken into account.

Overall the measurement results show the power of the multiline calibration technique, making it possible to model certain effects caused by the limitation of the printed circuit board processing. A better understanding of these limitations can lead to optimized design-rules and thus better end-user performance.

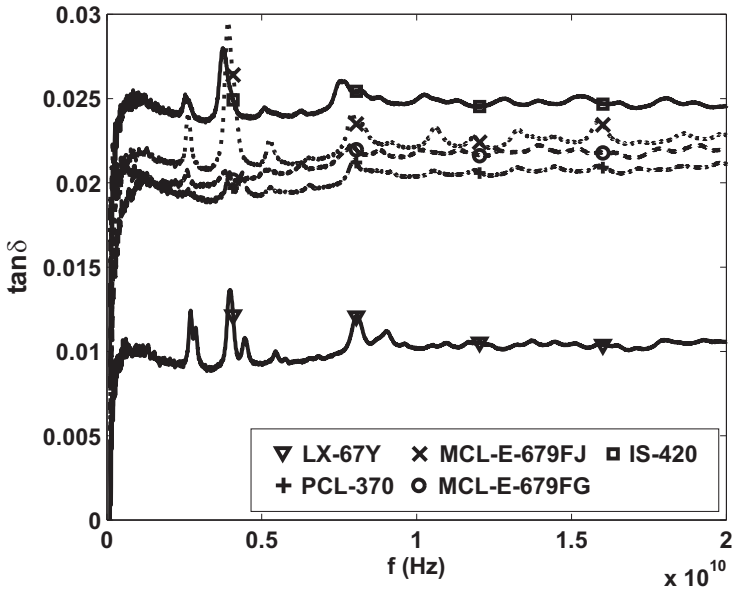


Figure 4.6: Frequency-dependent behaviour of the loss factor for the different printed circuit board materials

4.4.4 Conclusion

Development of new laminate materials and the introduction of high-speed applications into high volume processing extend the need for a practical wideband material characterization technique, which is easy to implement and reflects the real-life performance of printed circuit board designs. This research presents such a method based on multiline TRL calibration structures implemented on the final build-up of the printed circuit board. This powerful calibration method produces the propagation constant of the microstrip test structures, which can be used to extract the effective dielectric constant and loss factor. Simulations revealed the need for an adaptation of the conversion formula from the effective to the relative dielectric constant for the presence of a solder mask in combination with a high track thickness. Comparison of the resulting material parameters for different implementations gives a quantitative idea about the influence of solder mask, surface finish and glass fibre weave on the high-frequency performance.

Modern FR4 based materials offer reasonable high-frequency performance, however the dielectric loss can be too high for certain applications. High-frequency materials can be a valid alternative if the extra cost is justified, however special attention to surface finish, solder mask and glass fibres is needed

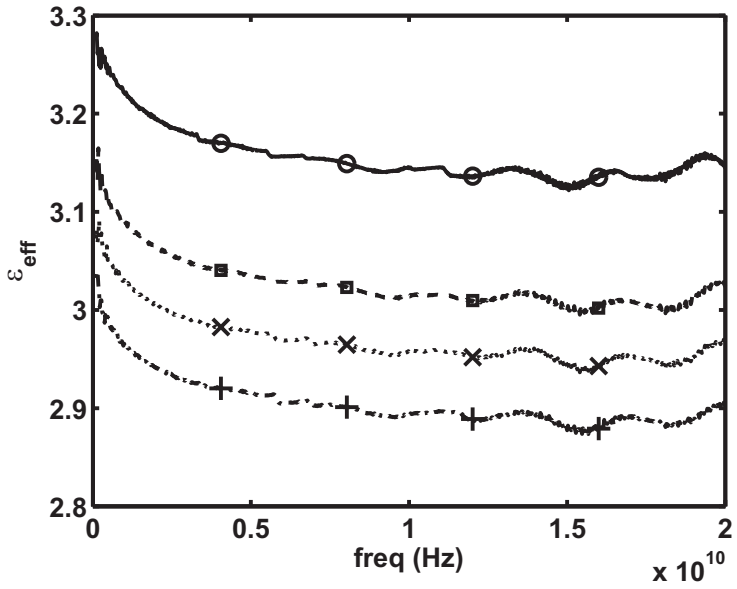


Figure 4.7: Frequency-dependent behaviour of the effective dielectric constant for the different test traces on the high-frequency material test board (o trace A, × trace B, □ trace C, + trace D)

in order not to undo the high-frequency advantages of these materials. High T_g and low CTE materials based on ceramic fillers not only suffer from high dielectric constants, but are marked by a high dielectric loss making these materials less suited for high-speed applications.

Based on the findings of this research, a quantification of the different effects of manufacturing decisions on laminate material, plating thickness, solder mask and surface finish can be integrated into the design process, accommodating the limitation of high-volume printed circuit board processing to the requirements of sufficient performance at high-frequencies.

4.5 Conclusion

In summary, the parameter extraction method starts by measuring the different line pairs. The measurement data is used as input for the multiline TRL calibration algorithm, resulting in the extraction of the propagation constant. The imaginary part of the propagation constant, the phase shift β, needs to be corrected for the skin effect, which requires the knowledge of the characteristic impedance of the microstrip. An iterative calculation, based on the

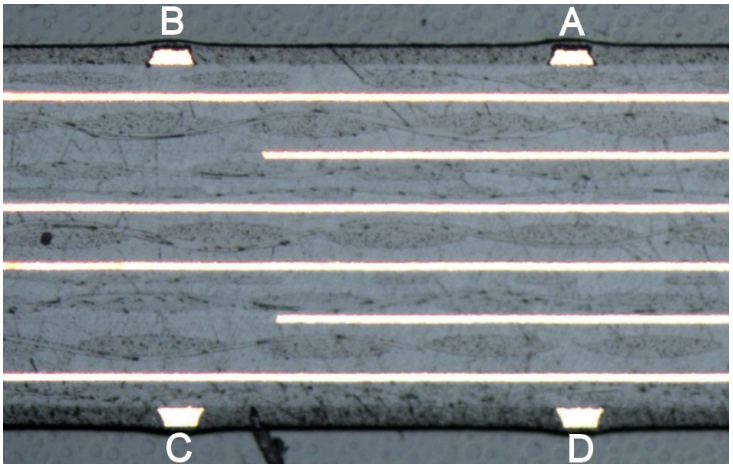


Figure 4.8: Cross section of the high-frequency material test board. Trace A is located on top of a fibre bundle, while trace B falls in between two bundles

capacitance of the microstrip, leads to the corrected value of the phase shift β, from which the effective dielectric constant of the microstrip is determined. After calculating the conductive loss, the effective value of the loss factor is extracted from the real part of the propagation constant. Using the adapted formula for the presence of the solder mask, the frequency-dependent behaviour of the dielectric constant and loss factor of the substrate material across the entire measured frequency range are revealed.

A fast and accurate method for the extraction of the material parameters is presented in this chapter. The strong point of the technique is the separation of the propagation constant extraction from the calculation of the material parameters. In this way, the propagation constant does not suffer from the approximations made in these formulae and the method is not limited to a specific application area. In the next chapter, the high-accuracy calibration algorithm will be used to determine the propagation constant of tracks running over embedded chips.

Chapter 5

Measurement results and discussion

Het leven is simpel. Het is de vaat doen. Een mens maakt borden vuil, wast ze schoon, wrijft ze droog, bergt ze weg, haalt ze weer uit de kast, maakt ze vuil, wast ze schoon, wrijft ze droog, bergt ze weg en haalt ze weer uit de kast, en op een dag valt de hele stapel uit je handen. (Uit "Godenslaap" van Erwin Mortier)

5.1 Measurement preparation

5.1.1 The radio frequency test vehicle

To verify the proposed model based on the theoretical analysis, a number of dedicated test structures are required. The model can be used to predict the effective dielectric constant, the characteristic impedance, the losses, and the per-unit-length parameters. The test structures need to allow the consistent and reliable extraction of all of these parameters. To minimize the introduction of difficulties that are not directly related to the parameter extraction, the test vehicle design needs to be kept as simple as possible. To determine the material parameters of the RCC, reference structures without embedded dies need to be included in the design. The propagation constant extraction based on the multiline TRL calibration procedure, as explained in chapter 4, fulfils all of these requirements.

Design

The aim of the test vehicle is to extract the propagation constant of traces running on top of embedded dies. The multiline TRL algorithm requires at least three, but preferably more, lines with identical propagation behaviour. To avoid difficulties with de-embedding of, for example, the part of the lines leading up to the chips, the entire length of the trace is placed above the chip. To achieve a good estimation of the propagation constant at low frequencies, lines of several centimetres long are required and thus a dummy chip of the same, or slightly longer length, is needed to obtain a valid result. Measuring the microstrip lines with coplanar probes requires an extra ground contact pad with associated ground via. Since the pitch of the coplanar probes is limited, the microstrips need to be placed close to the edge of the chip, as it is almost impossible to realize a ground via through the silicon. This also requires the ground vias to be placed close to the edge of the chip, resulting in extra restrictions for the alignment.

The test structures consist of single-ended microstrip lines and coplanar waveguides. The different lengths required for the multiline TRL calibration depend on the targeted frequency range and the available space. As stated in the previous chapter, calculating the line lengths is not straightforward. Following the suggestion by Marks et al. [77], the first line length difference was calculated to be a quarter wavelength at the centre frequency, and the second length difference is three times longer. Since for most of the conductivities the transition from slow-wave mode to dielectric mode occurs in the lower frequency range, the emphasis was placed on the lower half of the targeted frequency range (from 100 MHz to 20 GHz), and thus a "centre" frequency of 5 GHz was chosen. To calculate the quarter wavelength, the effective dielectric constant needs to be known. As seen from the modelling, this varies quite strongly over the frequency range. As a solution, the average effective dielectric constant was used, leading to a first length difference of 6 mm and a second length difference of 18 mm. Using a thru line of 2.5 mm, three line lengths are obtained: 2.5 mm, 8.5 mm and 20.5 mm. The effective phase difference for this combination of line lengths is obtained by calculating the phase difference for each line pair and using the maximum value at every frequency point. The result is plotted in Figure 5.1. Taking a minimum phase difference of 15° or 0.25 rad, the low frequency limit for these line lengths is about 400 MHz. By introducing an extra line of 44.5 mm, the low frequency limit can be moved to below 200 MHz. The improved effective phase difference is also plotted in Figure 5.1. Please keep in mind that these plots are not showing the limits of the frequency range, but only indicating possible frequency regions were the accuracy might be lower than expected (± 15° around multiples of 180°).

In addition to the lengths, the cross-section geometry of the test structures has to be synthesized as well. Both the microstrips and the coplanar waveguides

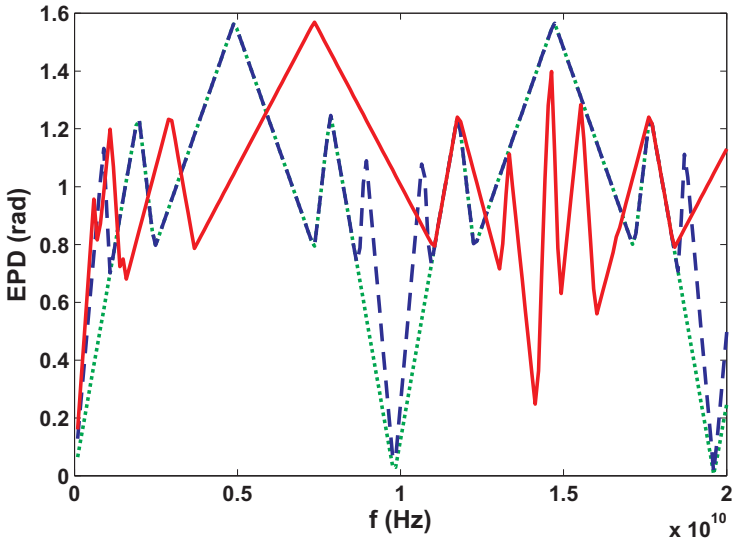


Figure 5.1: The effective phase difference for the lines used on RFTV-2006 and RFTV-2007. (·····) Thru (2.5 mm), Line 1 (8.5 mm) and Line 2 (20.5 mm); (- - - -) Thru (2.5 mm), Line 1 (8.5 mm), Line 2 (20.5 mm) and Line 3 (44.5 mm); (——) Thru (2.5 mm), Line 1 (6.5 mm), Line 2 (14.5 mm), Line 3 (35 mm) and Line 4 (65 mm)

are designed to be 50 Ω transmission lines. The effective dielectric constant used for the synthesis was that of the dielectric mode, which is the geometrical average of the three-layer dielectric sandwich[1]. This results in the following geometry for the microstrip: $w = 140\,\mu\text{m}$, $h_{RCC} = 20\,\mu\text{m}$, $h_{Si} = 50\,\mu\text{m}$, $h_{DAT} = 20\,\mu\text{m}$ and $t = 15\,\mu\text{m}$; and for the symmetrical coplanar waveguide: $w = 100\,\mu\text{m}$ and $s = 75\,\mu\text{m}$.

The radio frequency test vehicle (RFTV) consists of a 10 cm by 10 cm board with a 10 mm edge clearance. Placing all the different line lengths of microstrips and coplanar waveguides above the chip, resulted in a required chip surface of 80 mm by 10 mm. The microstrips are located 500 µm from the edge of the chip, corresponding to the pitch of the single-ended coplanar probes. The ground vias are placed about 150 µm from the edge to allow for sufficient alignment tolerance. The drill diameter of the via is 80 µm. The core layer consists of one continuous ground plane, so there are no fiducials present to align the chips during die bonding. Since all the test structures need to be positioned

[1]The synthesis of the geometry was performed before the multilayer model was finalised. Consequently, the correct slow-wave mode behaviour of a multilayer microstrip was not yet known. To avoid making the wrong assumptions, the effective dielectric constant of the dielectric mode was used.

relative to the chip boundaries, the corners of the total chip surface were used as alignment marks for the via drilling and copper structuring. Figure 5.2 shows the overall layout of the board, while Figure 5.3 shows a detailed drawing of the ground contact of the microstrip.

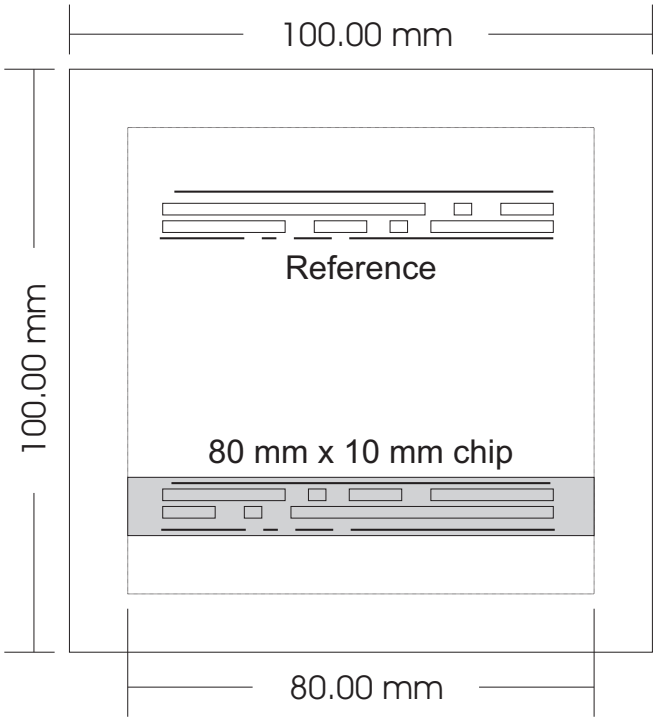


Figure 5.2: Layout for the radio frequency test vehicles (RFTV-2007 design), with the reference test structures at the top and the lines above the chip at the bottom

Measurement results of the first test boards without chips revealed the need for longer lines to obtain better results at lower frequencies. On the RFTV-2006 design, all of the lines, except the longest line were implemented twice for redundancy. With the new design, RFTV-2007, this redundancy was sacrificed for the use of additional, as well as longer lines. Figure 5.1 compares the effective phase difference of the old line lengths to the new line lengths (Thru (2.5 mm), Line 1 (6.5 mm), Line 2 (14.5 mm), Line 3 (35 mm) and Line 4 (65 mm)). The new line lengths show less peaks down to 0° or upwards to 180°.

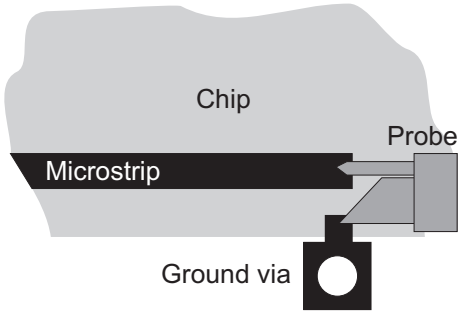


Figure 5.3: Detail of the probe contacts on RFTV. Due to the small pitch of the probes (500 µm) both the microstrip line and the ground via need to be placed close to the edge of the chip

Manufacturing

The process flow for the radio frequency test vehicle is a simplified version of the process for embedding active components in printed circuit boards described in chapter 2. The major steps of the flow are placement of the chips, lamination of the RCC, drilling and metallizing the via and finally structuring the copper. During several of these steps issues arose, causing the need for workarounds, design changes and new process runs.

Since the test chips consist of dummy silicon dies, the wafer preparation is limited to thinning down to 50 µm, applying the die attach tape and dicing. The requirement of very long chips created an additional difficulty, since standard die bonding equipment can not handle these chips. An initial solution was to place several smaller chips next to each other, aligning each chip to perfectly touch the neighbouring chip. The placement of eight 10 mm by 10 mm dies was done in-house using a flip-chip bonder to place the chips and a Farco thermocompression bonder to secure the chips to the substrate. The flip-chip bonder offers a simultaneous view of the chip that needs to be placed and the bonding position. By moving the targeted bonding position to the space adjacent to the previous chip, a continuous row of chips can be formed. After placing each chip, the substrate is moved to the thermocompression bonder, where a heated thermode is pressed onto the chip to liquefy the die bonding tape and to fix the chip to the die bonding position. The applied pressure should not be too high, to avoid squeezing out the die bond adhesive from underneath the chip (3 min at 120 °C and 1 bar). Unfortunately, both during the transport from the flip-chip bonder to the thermocompression bonder and during the thermocompression setup, slight movement of the chips is observed, causing misalignment of each chip. At the end of the row, this results in a severe offset of the chip corners, making it almost impossible to correctly align

the mask to the substrate. To solve this issue, a single piece of silicon of 8 cm by 1 cm is used for the following process runs. This required the thinning and dicing of a new (dummy) wafer, which was done at Disco HI-TEC by order of TU Berlin. Picking these chips from the wafer and placing them on the substrate is done by hand using extreme caution not to damage the chips. The exact location and angle of the chip is not so critical, since all other structures and process steps are aligned to the chip. The substrates are then placed into an oven with a thick steel plate on top to ensure a good adhesion of the chips to the board (1 h at 160 °C).

A visual inspection before lamination revealed that small cracks are sometimes present after die bonding. Since the chip is just dummy silicon and not functional, this is not believed to have any significant influence on the measurements. The Hitachi MCF6000E RCC used for the HIDING DIES project was discontinued and replaced by the Isofoil 160i from CircuitFoil FC with a resin thickness of 90 µm and a 5 µm copper foil. Since the glass transition temperatures of both materials are similar, the same lamination profile used at the end of the HIDING DIES project is also used for RFTV. Cross-sections and 3D profile measurements revealed that there is a large difference in total height between the areas above the chip and the areas next to the chip. This is an indication of insufficient flow of the resin during lamination. To increase the flow, a higher starting temperature (110 °C instead of 80 °C) is used in combination with a faster heating rate (9 °C/min versus 6 °C/min). The higher starting temperature causes the resin to melt earlier in the lamination cycle, while a faster heating rate gives the resin less time to cure during heating. To make sure that the resin is fully cured, the temperature is held at its maximum value for an additional 20 min. A comparison of the lamination profiles can be found in Figure 5.4.

Since there were reliability issues when using the trepanner on the YAG laser system, wet etching with a dedicated via masks was used to open the copper on the first runs. The resin is then removed with the CO_2 laser, using the via openings as ablation mask. Due to the small openings around the fiducials on the glass mask, there was insufficient light falling onto the boards. Using the microscope of the aligner, the corners of the chips could not be distinguished from the underlying board substrate and thus it was not possible to align the mask to the board. The solution was to change the design of the fiducials on the mask. Instead of a rectangular shape to fit to the corner of the chip, a cross with an enlarged opening around the fiducial is used to allow more light to pass through, offering a better visibility of the corners of the chip (Figure 5.5). With the installation of a new trepanning system, mask alignment is only needed for the structuring of the top layer.

The biggest problems however were encountered with the metallization of the vias. After the vias are drilled, they are metallized by first swelling and

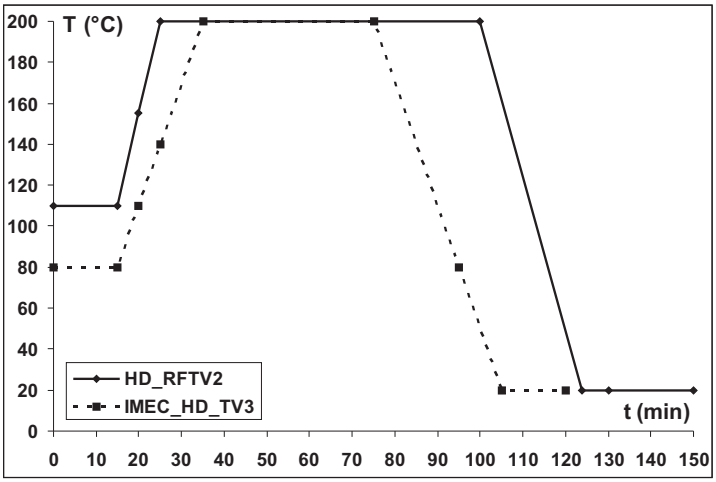


Figure 5.4: Comparison of the temperature profile of the lamination cycle used for RFTV2 (IMEC_HD_TV3) and RFTV3 (HD_RFTV2). Notice the higher starting temperature and the faster heating rate of the HD_RFTV2 profile

etching the holes, followed by the deposition of a seed layer by electroless copper plating. Finally, the galvanic copper plating deposits 10 µm to 15 µm inside the via. The deposition of a continuous seed layer is very critical. The most important process parameters are the conditioning of the epoxy surfaces to ensure a good wettability and the plating time of the electroless copper bath. If the height of the via is higher than the drill diameter, the via is said to have a high aspect ratio. This hinders the replenishment of the electroless copper plating solution at the lower parts of the via, leading to the depletion of the copper ions in that area. As a result, the bottom part of the vias is not plated and the via fails to make contact (Figure 5.6(a)).

A total of five process runs over a period of two years were needed to obtain a fully functional test vehicle. The first run (RFTV1) used the RFTV-2006 design with the eight 10 mm by 10 mm dies in a row and could not be finished because of the misalignment after die bonding. For the following run (RFTV2), a new wafer with long dies in one piece was ordered. The RFTV2 run revealed that the height of the RCC above the chip was much larger than anticipated (60 µm instead of 20 µm). The via drill diameter of 80 µm resulted in an aspect ratio of almost 2 : 1, which was too high for the plating process. A new design (RFTV-2007) featured enlarged microvia drill diameter (120 µm) and improved alignment marks, to solve the visibility issues of the alignment marks. In combination with the optimized lamination profile, the aspect ratio was now closer to 1 : 1, but remained insufficient for reliable via metallization during

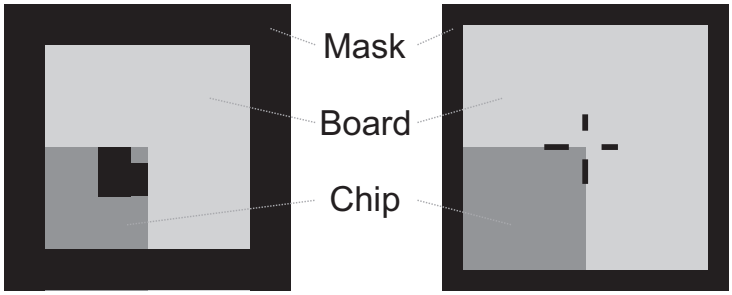


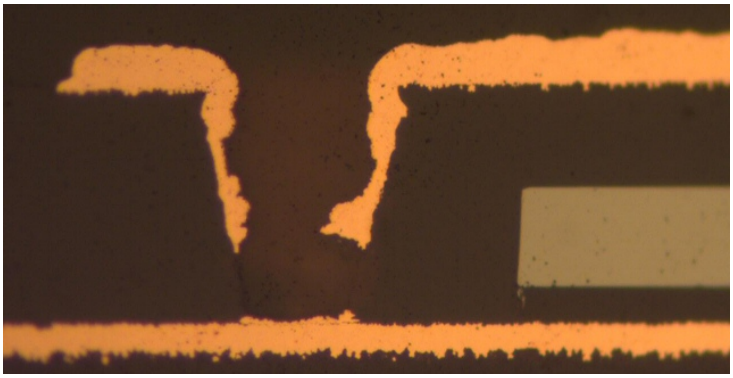
Figure 5.5: Fiducial design for RFTV-2006 and RFTV-2007. Since there are no copper structures on the core, the masks are aligned to the corners of the chip. For the RFTV-2006 design (left), this was done using a rectangular shape, while the RFTV-2007 design (right) uses a more convenient cross shape

the third process run (RFTV3). The via metallization for a fourth process run (RFTV4) was outsourced to TU Berlin, who use a direct metallization process with a conductive palladium seed layer. The result was better, but still not satisfactory.

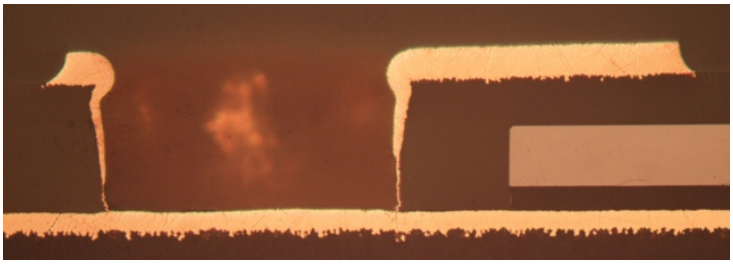
To prevent further loss of test boards with embedded chips, a thorough investigation of the plating process was performed. The outcome of the parameter study was an optimised conditioning time, a prolonged plating time for the electroless copper bath (from 25 min to 60 min) and a suggested minimum aspect ratio of 1 : 2. Another design revision (RFTV-2009), including vias of 250 µm drill diameter, was implemented and additional wafers were ordered. The first four boards of the run (*RF51* to *RF54*) use RCC with a base thickness of 70 µm, while the remaining boards (*RF55* to *RF58*) employ a base resin thickness of 90 µm. This results in a variation of the height of the RCC layer above the chip. Six of the eight processed boards of run RFTV5 showed good metallization results (Figure 5.6(b)). The RF54 board suffered from a bad coverage of the electroless seed layer, while the RF57 board was damaged during the electroplating process. Finally, when structuring the boards by wet etching, an additional board (RF58) was lost due to insufficient coverage of the photoresist over the large microvias. The remaining five boards are used for the measurements.

5.1.2 Measurement setup

The multiline TRL algorithm requires the cascade (or T-) parameters of the lines on the test board as input. These can be converted from S-parameters, which are measured using a vector network analyser. A dedicated measurement setup is used consisting of an optical table with orthogonal rails that allow



(a) RFTV3 - bad via contact



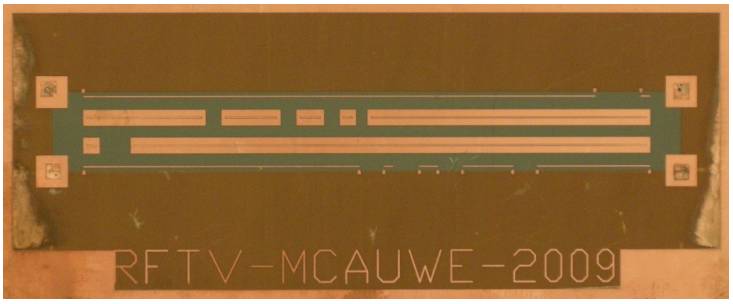
(b) RFTV5 - good via contact

Figure 5.6: Metallization of ground vias for the third and the fifth process run. Notice the large difference in aspect ratio

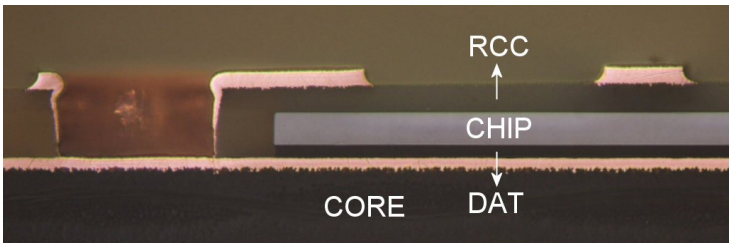
the probe holders to be placed almost anywhere on the table surface. Both very short (< 1 mm) and very long (up to 50 cm) lines on large printed circuit boards can be contacted using this setup. The probe holders can accommodate a number of different coplanar microwave probes, which realise the transition from the coaxial cable to a coplanar pin layout. This avoids the need for extra adapters on the test board and minimizes the influence of the probe contacts on the device under test.

For the RFTV test vehicle, the test structures are contacted using Picoprobe 50A-GS/SG-500-P probes, with a single ground-signal configuration and a pitch of 500 µm, certified up to 50 GHz. The probes are connected to the network analyser with 2.4 mm coaxial cables. The Agilent PNA 8364B vector network analyser is capable to measure from 10 MHz up to 50 GHz, but the frequency range here was limited to 100 MHz - 20 GHz.

A number of calibration substrates are available using different calibration techniques. Since it is more practical than TRL and it has a higher accuracy



(a) The design includes microstrips and coplanar waveguides on top of an embedded die



(b) The cross-section shows the multilayer microstrip on the right and the ground contact with microvia next to the chip on the left

Figure 5.7: Layout and cross-section of the measurement test structures

than SOLT (*Short-Open-Load-Thru*), a planar LRM (*Line-Reflect-Match*) calibration is performed to compensate for internal errors of the network analyser and the cables. Instead of using several line standards of different lengths to cover the complete frequency range in a full TRL calibration, a *Match* standard is used to simulate an infinitely long line [2]. As a result of the calibration, the reference plane is shifted to the probe tips.

5.2 Measurement results

5.2.1 Geometrical and material parameter extraction

To calculate the RLGC parameters using the proposed model, both the geometrical and material parameters need to be known as accurately as possible.

[2]Since the choice in calibration technique is limited to the available standards on the commercial calibration substrate, the multiline TRL calibration was not an option for the probe tip calibration. Implementing custom calibration substrates manufactured in-house was investigated, but proved not to be worthwhile.

Table 5.1: Overview of the measured geometrical parameters of the RFTV5 boards for the reference test structures (*REF5X*) and the microstrips running above the chip (*RF5X*). All dimensions are in µm

Board	w	h_{RCC}	h_{Si}	h_{DAT}	t
REF51	149.91	78.16			23.8
REF52	147.44	78.16			22.9
REF53	145.01	78.16			22.1
REF55	144.60	93.44			21.6
REF56	148.17	93.44			22.9
RF51	151.76	49.58	50.77	21.49	23.7
RF52	152.71	49.58	50.77	21.49	23.3
RF53	145.70	49.58	50.77	21.49	22.7
RF55	144.10	60.92	52.09	21.86	22.0
RF56	150.30	60.92	52.09	21.86	23.4

A first estimate for these parameters can be found in the design and the material data sheets, respectively. Manufacturing tolerances, however, can lead to significant deviations from the targeted geometry and the information from material data sheets is either very scarce or not specific enough. As a result, these parameters should be verified using measurements as much as possible.

The geometrical parameters, such as trace width and thickness and the height of the different layers, are obtained by making cross-sections of the board. Due to the diverse hardness of the applied materials, an improved polishing process was developed, applying lower pressure in combination with dedicated grinding solutions. After polishing, the distances are measured using a high resolution inspection microscope (*Nikon Optiphot 200*) and a digital image capture system (*Nikon DS camera and NISElements software*). Two boards, one for each base resin thickness, are sacrificed for cross-sectioning: RF54 and RF58. The first board suffered from several bad via contacts, while the latter board was damaged during etching and thus both boards could not be used for measurements anyway. The measured height of the different layers was employed for all the related test boards. In addition, the width and the thickness of the microstrip trace are measured for each board individually with the microscope and a Tencor profilometer. Table 5.1 gives an overview of the measured geometrical parameters, which are averaged across the different lines. Variations from board to board of 5 % for the width and 10 % for the thickness of the trace are observed.

The conductivity of the silicon was measured before thinning by means of a four-point-probe method (Veeco instruments FPP5000). All four wafers had a comparable conductivity of about 10 S/m. Because of the broad frequency

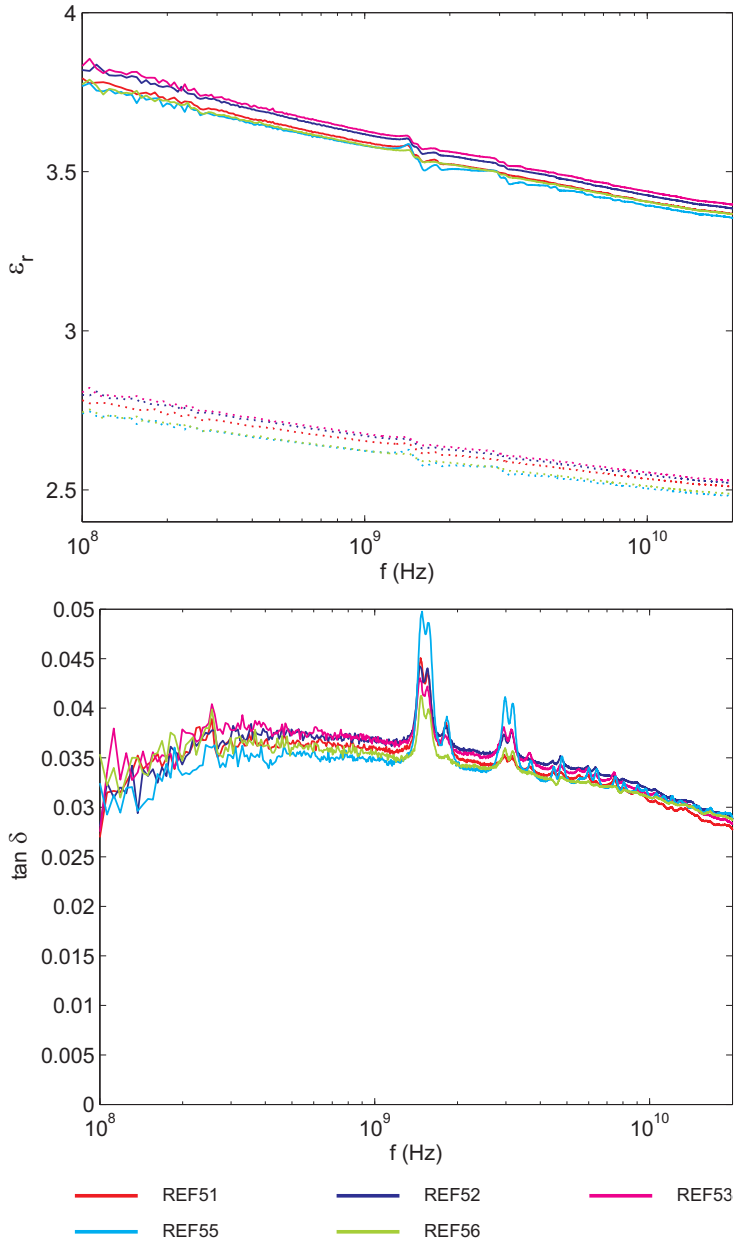


Figure 5.8: Extracted material parameters for the RCC. Both the effective (dotted line) and the relative (full line) dielectric constant are presented

range, the variation of the dielectric material parameters with frequency needs to be known. For the silicon chip, the frequency dependency of the dielectric constant is negligible, while for the die attach tape only a value of 2.94 at 1 MHz could be found in the data sheet. The latter could not be confirmed by separate measurements, since the material is not available individually.

The dielectric constant and loss tangent of the RCC are determined using the methodology for parameter extraction described in chapter 4. The reference structures, that are identical to the test structures running above the chip, are measured and the data is used as input for the ML-TRL algorithm. The extracted propagation constant is then used to calculate the dielectric constant ϵ_{RCC} and the loss tangent $\tan\delta_{RCC}$. Figure 5.8 shows the results for both ϵ_{RCC} and $\tan\delta_{RCC}$. Both the effective (dotted line) and the relative (full line) dielectric constant are presented. The relative dielectric constant varies more than 10 % over the entire frequency range, which confirms that the frequency dependence of the material parameters can be significant. The resonant peaks in the loss tangent, also present as small riples in the dielectric constant, occur when the length of the longest lines becomes equal to $\lambda/2$. According to the Circuitfoil data sheet, the dielectric constant and loss tangent at 1 GHz are 3.44 and 0.03 respectively. The extracted material parameters are slightly higher, but correspond well to these values.

5.2.2 Propagation constant comparison

With all geometrical and material parameters known, the proposed model can be used to calculate the effective dielectric constant, the characteristic impedance, the losses, and the per-unit-length parameters for the microstrips above the embedded die [3]. To avoid the need for additional manipulations of the measurement data, the comparison between the model and the measurements is performed using the propagation constant. For the measurements, the propagation constant is extracted using the multiline TRL algorithm, while the per-unit-length RLGC parameters from the model can be used to calculate the modelled propagation constant.

$$\gamma = \alpha + j\beta = \sqrt{[R(\omega) + j\omega L(\omega)]\,[G(\omega) + j\omega\, C(\omega)]} \tag{5.1}$$

From the phase shift β, the effective dielectric constant ϵ_{eff} is calculated to allow a more comprehensible presentation of the results. Figure 5.9 compares the measurements to the model for the effective dielectric constant and the total loss. The ripples in the modelled results are caused by the resonances in the extracted material parameters. With a silicon conductivity of 10 S/m, the propagation mode at low frequencies is the slow-wave mode. At frequencies

[3] Since the model cannot predict the parameters of the coplanar waveguides, no further evaluation of the coplanar waveguide test structures is performed.

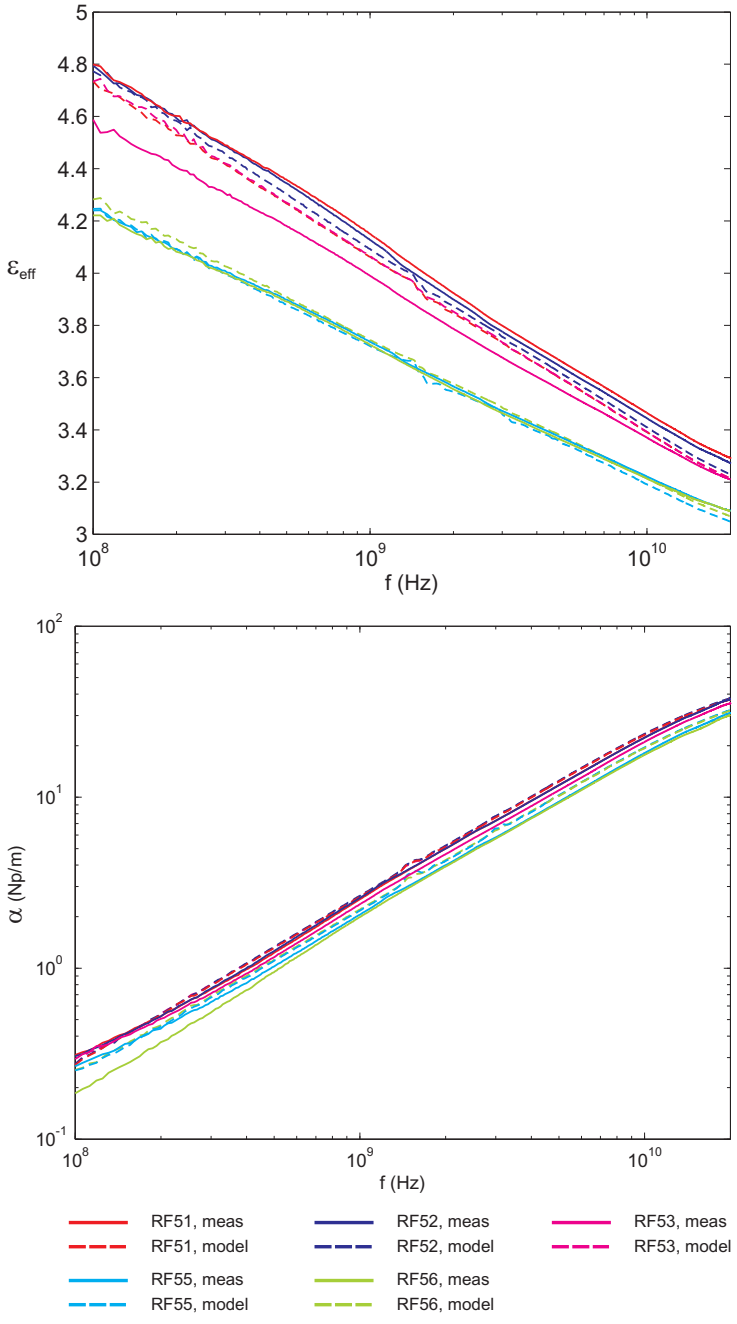


Figure 5.9: Comparison of the measurement results to the model

above 5 GHz, the multilayer microstrip starts to transition to the dielectric mode. The typical relaxation behaviour is less clear due to the substantial frequency dependence of the RCC parameters. The variation of the effective dielectric constant over the entire frequency range is more than 30 %, so the effect of the silicon is still pronounced. The beginning of the dielectric region is indicated by the slight decrease of the slope of the loss at the highest frequencies (> 10 GHz). The effective dielectric constant for the RF55 and RF56 boards is lower due to the higher base thickness of the RCC used for these boards and thus the influence of the silicon layer is proportionally smaller. This is also reflected in the reduced frequency dependence.

Overall, there is a good agreement between model and measurements. A detailed error analysis is performed in section 5.3.1.

5.2.3 Measurement results of the HIDING DIES test vehicle

Prior to the design and manufacturing of a dedicated high-frequency test vehicle, a number of RF test structures were included in the technology evaluation test vehicle (TV1) of the HIDING DIES project. The test structures consist of microstrip lines running partially above an embedded die. Five microstrips of 2 cm long are located above a 10 mm by 10 mm dummy chip. The width of the different microstrips is varied to verify the influence of the impedance step on the signal propagation and two of the five lines have a reduced width above the chip to minimize the reflections. Details of the geometry can be found in appendix B. Note that the synthesis of the geometry was performed at a very early stage, both technology-wise as from a RF modelling point of view, so the details of this synthesis will not be further discussed. The measurement results are presented here as an extra verification of the proposed model.

The S-parameters of the microstrip passing over an embedded chip are calculated by means of a circuit simulator (Agilent ADS). The parts of the microstrip next to the chip are modelled using the proprietary microstrip model of the simulator, which is based on well-known empirical formulas. The multilayer microstrip above the die is inserted as a black box component, for which the frequency dependent RLGC parameters are generated using the proposed model. The material parameters for the Hitachi RCC ($\epsilon_{RCC} = 4.2$, $\tan\delta_{RCC} = 0.03$), the silicon die ($\epsilon_{Si} = 11.8$, $\sigma_{Si} = 5$ S/m) and the die attach tape ($\epsilon_{DAT} = 3$) are based on the respective data sheets and, where possible, verified through reference test structures without chips. Figure 5.10 shows the amplitude and phase of the calculated S-parameters for a 275 µm wide and 32 µm thick microstrip trace. The height of the substrate is 100 µm, which is divided into 20 µm RCC, 60 µm silicon and 20 µm tape for the part above the chip. Overall, the model agrees very well with the measurements. The differences can be explained by

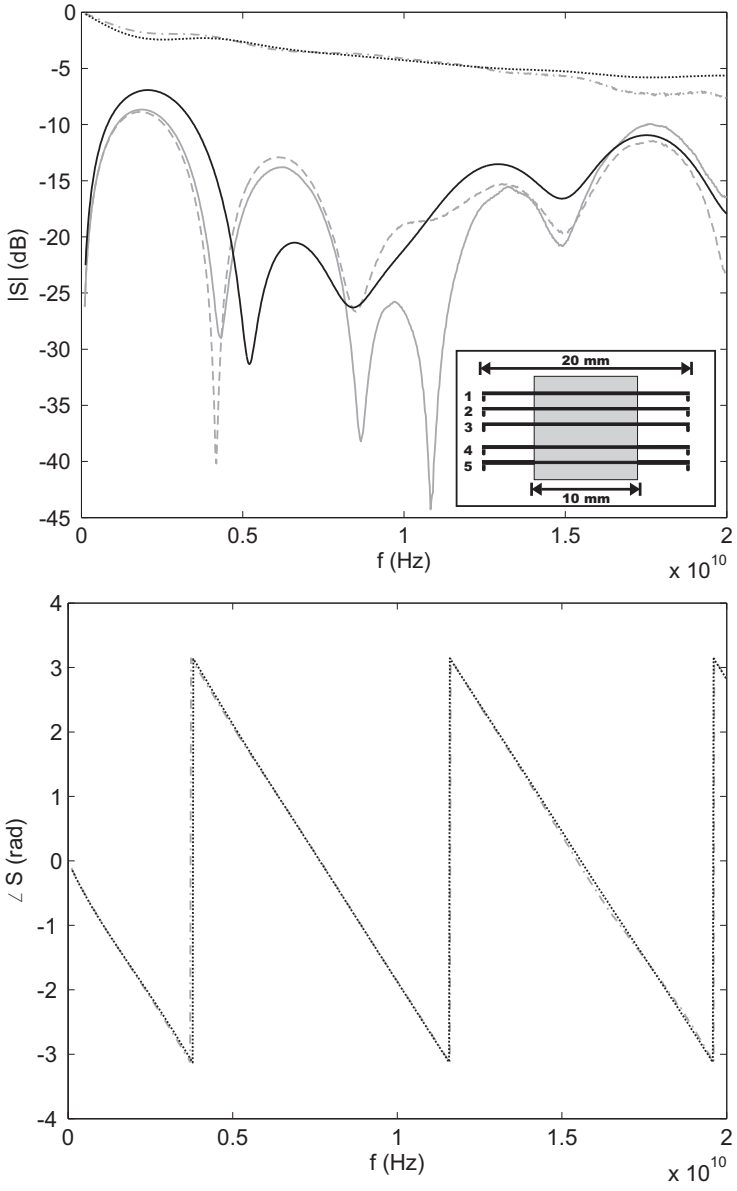


Figure 5.10: Calculated S-parameters for a microstrip test structure running over an embedded die. (——) S_{11} (model); (·····) S_{21} (model); (——) S_{11} (measured); (- - - -) S_{22} (measured); (-·-·-) S_{21} (measured)

the missing frequency-dependent information and the overall uncertainty of the material parameter values. The underestimation of the loss at high frequencies by the model is likely due to the Ni/Au surface finish of the test samples. The microstrips with different width showed similar behaviour and it was also observed that the step in width above the chip did not dramatically improve the reflection. These results indicate that the output of the model can easily be implemented in existing circuit simulators to accurately predict the behaviour of microstrip lines running over embedded dies.

5.3 Discussion

5.3.1 Error analysis for material and geometrical parameters

To understand the differences between the measurements and the model, a closer look at the influence of the material and geometrical parameters can be interesting. The uncertainty of these input parameters has a direct influence on the accuracy of the modelling results. Geometrical parameters are determined by measuring cross-sections, which are quite accurate ($\pm 1\,\mu$m); however, manufacturing tolerances introduce variations in track width, substrate height and track thickness along the line. Material parameters can be found in material data sheets or extracted from measurements using dedicated methodologies. The dielectric constant and loss tangent of the RCC are determined using the methodology for parameter extraction described in chapter 4. The conductivity of the silicon is measured using a four-point-probe method, while other parameters, such as the dielectric constant of the silicon and the adhesive (DAT), could only be taken from the data sheet.

The parameters reflecting the geometry and materials of the RFTV are used as a reference for this investigation. Each parameter is changed over a small range and the relative deviation from the reference results is calculated. The amount of change is based on the observed variations of the geometrical parameters during cross-section measurements and the expected uncertainty of the material parameters. The material parameters extraction of the RCC is very accurate, so an arbitrary variation of ± 10 % is introduced here to see the corresponding influence on the results.

The propagation constant is calculated for all variations and used to determine the relative deviation in effective dielectric constant (derived from the imaginary part of the propagation constant) and the total loss (real part of the propagation constant). The results are shown in Table 5.2, revealing the maximum deviation over the entire frequency range (100 MHz to 20 GHz). The deviation in characteristic impedance is not presented in the table, since it

Table 5.2: Influence of changing geometrical and material parameters on the modelled results

Parameter	Reference	Deviation	$\Delta\epsilon_{eff}$ (%)	$\Delta\alpha$ (%)
ϵ_{RCC}	$3.5(1-j0.03)$	± 10 %	± 8.5	± 9.9
ϵ_{Si}	11.8	$11.5 \rightarrow 12.5$	$-0.1 \rightarrow 0.3$	$-4.2 \rightarrow 1.9$
σ_{Si}	10	$8 \rightarrow 12$	$-1.6 \rightarrow 1.3$	$-9.4 \rightarrow 6.7$
ϵ_{DAT}	3	$2 \rightarrow 4$	$-6.1 \rightarrow 3.7$	$-9.6 \rightarrow 15.7$
w	150 µm	± 10 µm	$-1.8 \rightarrow 1.7$	$-2.0 \rightarrow 1.9$
h_{RCC}	50 µm	± 5 µm	$-4.6 \rightarrow 5.5$	$-8.8 \rightarrow 10.6$
h_{Si}	50 µm	± 2 µm	$-0.5 \rightarrow 1.0$	± 2.6
h_{DAT}	20 µm	± 2 µm	± 0.6	$-4.0 \rightarrow 3.8$
t	25 µm	± 3 µm	± 0.6	$-1.7 \rightarrow 2.0$

shows a similar behaviour as the effective dielectric constant, although the deviation is not as large. Overall, the deviations of the results are smaller than the variations of the input parameters (sensitivity < 1), but the total loss seems to be more sensitive to the input parameters than the effective dielectric constant. Note that both the dielectric constant and the loss tangent of the RCC are changed at the same time, resulting in quite a large deviation in total loss. The most critical input parameters are the height and dielectric constant of the RCC. This also means that the manufacturing tolerances for the height of the RCC above the chip need to be very tight to assure a controlled impedance. This is even worse when the RCC layer above the chip becomes thinner (< 20 µm), and thus small variations can cause large deviations in characteristic impedance. In addition, there can be a significant difference in resin height between the middle of the chip and the edge for large chips (10 mm by 10 mm). The total loss is in general quite sensitive to the material parameters and thus more difficult to model. Since there is no information available about the loss tangent of the adhesive, it was not included in the propagation constant comparison. When a loss tangent of 0.03 for the adhesive is added, the overall loss increases with only 5 %, because, for this frequency range, the dielectric loss is much smaller than the loss in the silicon.

It is clear that these deviations show a strong dependency on frequency. For example, the influence of the height and the dielectric constant of the silicon will be small in the slow-wave mode. On the other hand, the conductivity of the silicon will have a distinct effect on the loss in the dielectric mode. Figure 5.11 shows the frequency dependency of the relative deviation of the results for the parameters of the RCC and the adhesive. The effect of changing the material parameters of the adhesive on the total loss shows a strong dependence on frequency. However, because of the large variation of the input parameter

(±33 %), the influence is slightly exagerated here. The sensitivity of the effective dielectric constant to the height and dielectric constant of the RCC is close to 1 and decreases slightly with frequency (5.11(a)). The parameters of the RCC almost completely dominate the effective dielectric constant in the slow-wave region, but the influence on ϵ_{eff} is spread proportionally over the three materials for the dielectric mode. This is also reflected in the sensitivity of the effective dielectric constant to the parameters of the adhesive, which is small in slow-wave mode and increases towards the dielectric region (5.11(c)). Increasing the dielectric constant of the adhesive or decreasing the height, extends the slow-wave region to higher frequencies and thus the total loss for a given frequency is reduced. However, the increase in effective dielectric constant towards the dielectric mode results in higher loss at high frequencies (5.11(d)). Both the dielectric constant and the loss tangent of the RCC are changed at the same time, resulting in a combination of increased dielectric loss due to the higher loss tangent and a minor dependency on frequency as an effect of the transition to the dielectric mode (5.11(b)).

Based on this analysis, a more detailed look at the difference between measurements and the model is undertaken. The extracted propagation constant is used as a reference to calculate the relative error of the modelled results.

$$\Delta\gamma = \frac{\gamma_{model} - \gamma_{meas}}{\gamma_{meas}} \tag{5.2}$$

The relative error for the effective dielectric constant and the total loss is depicted in Figure 5.12. The agreement for ϵ_{eff} is better than ±4 % over the entire frequency range, while the loss corresponds within about ±15 %, except for the RF56 board. The frequency dependence of the relative error of the dielectric constant is similar for all boards, although the curves seem to be offsetted with regards to each other. This is also visible for the relative error of the loss. Looking at $\Delta\epsilon_{eff}$ for the RF53 board, a slow decline with frequency can be observed. When comparing this to Figure 5.11(a), the cause can either be an overestimation of the dielectric constant of the RCC or an excessive height of the RCC layer used for the modelling. Since the measured dielectric constant for the RF53 board agrees well to the values for the other boards (see Figure 5.8), the height of the RCC is suspected to be wrong. To verify this hypothesis, additional cross-sections of the RF53 board are performed, which indeed reveal a slightly increased height of 50.49 µm. This 2% difference in height reduces the maximum relative error for the effective dielectric constant of the RF53 board from 3.5% to 2% and has a similar effect on the error of total loss.

Another peculiarity can be seen in the loss of the RF56 board at low frequencies. There is a huge discrepancy between the model and the measurements, as the measured loss is far lower than the modelled loss. This is not present for the other boards, nor is it reflected in the relative error of the dielectric con-

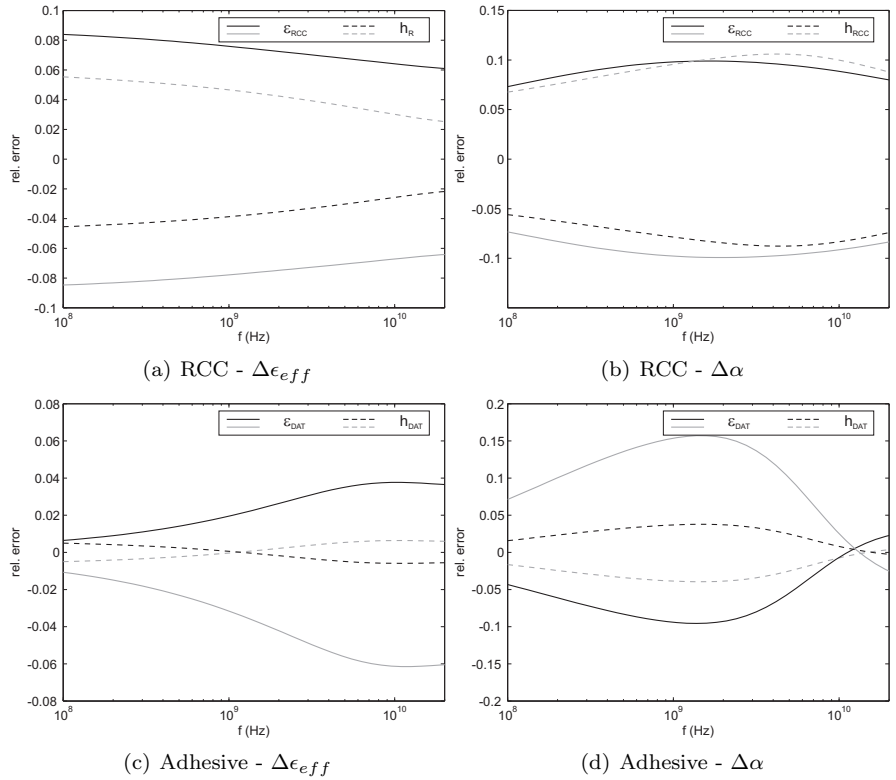
stant. Since the issue occurs at low frequencies, additional DC measurements are performed to single-out the problem. The microstrip traces show no apparent decrease in resistance, but some of the ground contacts reveal an excessive resistance, possibly caused by insufficient copper plating inside the microvia. Looking back at the multiline TRL algorithm, the measured S-parameters are converted to cascade parameters and combined into a line pair matrix (M_{ij}). All elements of this matrix have a common $1/\left(S_{21}^{j}S_{12}^{i}\right)$ factor. An increased ground resistance leads to a higher insertion loss and thus a common reduction of the elements of M_{ij}. As a result, the calculated eigenvalues are lower and the extracted loss is reduced. The imaginary part of the propagation constant remains unaffected.

Without these exceptions, the overall accuracy of the model is within ± 2 % for the effective dielectric constant and around ± 10 % for the loss.

In chapter 3, the accuracy of the proposed model was determined by comparing the RLGC parameters to the simulation results. The resistance and conductance per-unit-length showed some discrepancies between model and simulations. The measurement results present an additional reference to verify the validity of the model and the simulations. Figure 5.13 shows the effective dielectric constant and the total loss and their respective relative errors for the RF52 board. The effective dielectric constant exhibits a maximum error of 2 % for both the model and the simulations. The biggest difference is situated at the centre of the frequency range, which is where the transistion from the slow-wave mode to the dielectric mode begins. Neither the model nor the simulation accurately predicts the loss of the multilayer microstrip. The logarithmical scale used for the total loss gives the impression that the model and simulation agree well to the measurements. However, the relative error reveals discrepancies of up to 8 %. The difference between the model and the simulation becomes larger as the frequency increases. At high frequencies, the modeled loss is about 5 % higher than the mesurements, while the simulation results remain about 2 % to 4 % below the measurements. The model seems to overestimate the loss of the multilayer microstrip, but is slightly more accurate in predicting the effective dielectric constant.

5.3.2 Eye diagram analysis

So far the focus has been on the behaviour in the frequency domain of the extracted parameters and the resulting S-parameters. The performance of digital systems is often verified using time domain simulations, since this gives a better representation of the real-world behaviour. A useful tool for the qualitative analysis of signals used in digital transmission is the eye pattern or eye diagram. By providing an at-a-glance evaluation of the system performance, the eye diagram offers insight into the nature of channel imperfections. Care-



(a) RCC - $\Delta\epsilon_{eff}$

(b) RCC - $\Delta\alpha$

(c) Adhesive - $\Delta\epsilon_{eff}$

(d) Adhesive - $\Delta\alpha$

Figure 5.11: Frequency dependence of the influence of changing geometrical and material parameters on the effective dielectric constant and the total loss. The black lines correspond to an increase of the input parameter, the grey lines reflect a decreasing input parameter

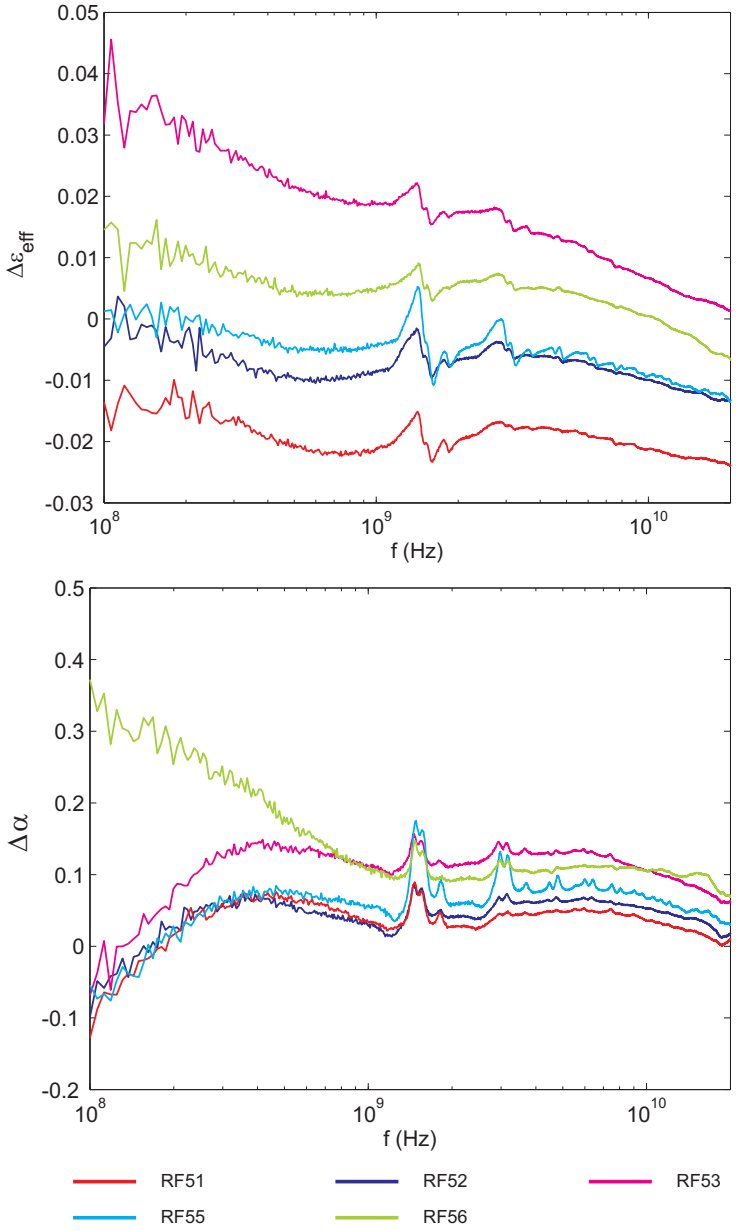


Figure 5.12: Error analysis for the modelled propagation constant versus the propagation constant extracted from the measurements

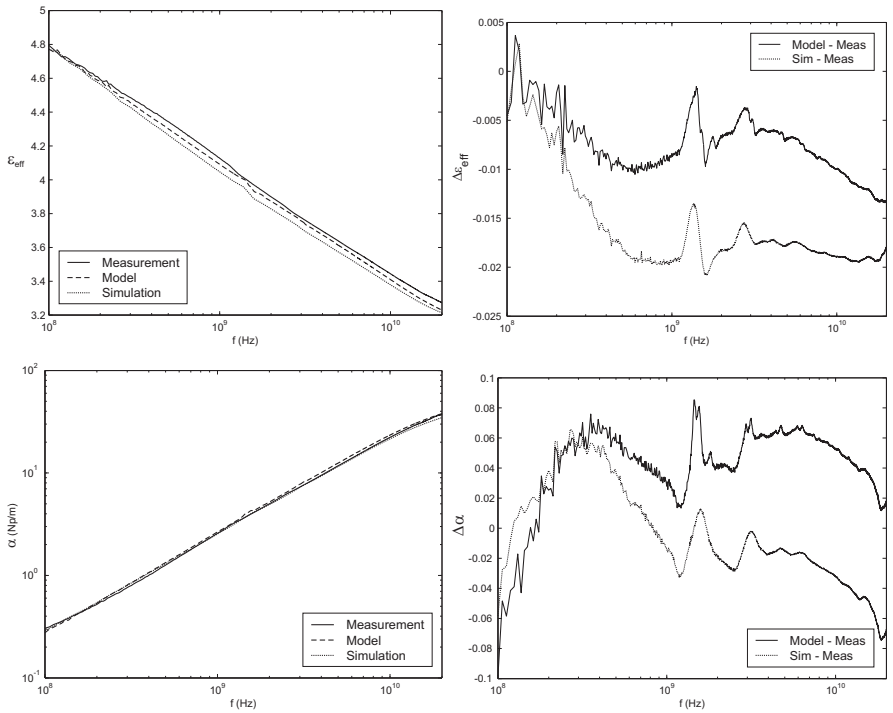


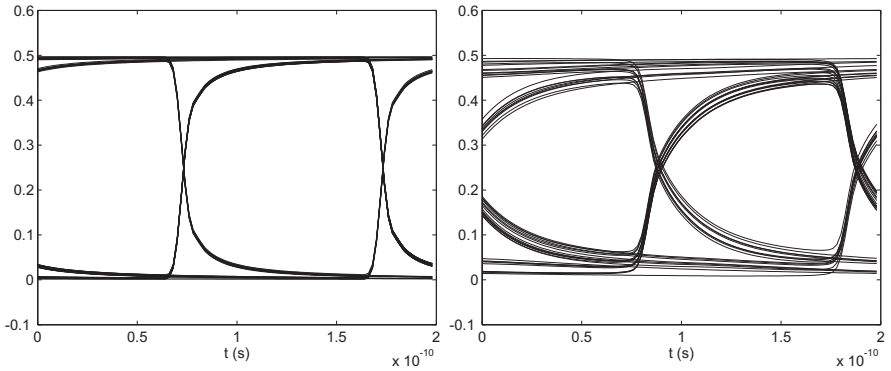
Figure 5.13: Comparison of the proposed model and the quasi-static simulations to the measurement results for the RF52 board

ful analysis of this visual representation leads to a first-order approximation of signal-to-noise ratio, clock timing jitter and skew. To obtain the eye diagram, a pseudo-random bit stream is generated and used as input to the system under test. The time domain signal at the output is converted into an eye diagram by overlapping the different bit periods.

The system under test for this investigation is a microstrip passing over an embedded chip, consisting of three section of 10 mm as shown in Figure 5.14(e). The first and last sections of the interconnection are microstrip lines with a 90 µm RCC substrate ($\epsilon_{RCC} = 3.5$, $\tan\delta_{RCC} = 0.03$). The multilayer microstrip in the middle represents the part of the trace running over the chip ($h_{RCC} = 20\,\mu m$, $h_{Si} = 50\,\mu m$ with $\epsilon_{Si} = 11.8$, and $h_{DAT} = 20\,\mu m$ with $\epsilon_{DAT} = 3$). The frequency-dependent RLGC parameters for the multilayer microstrip are generated using the proposed model and used as black box component for the simulation, while the microstrip lines use the proprietary model of the circuit simulator (Agilent ADS).

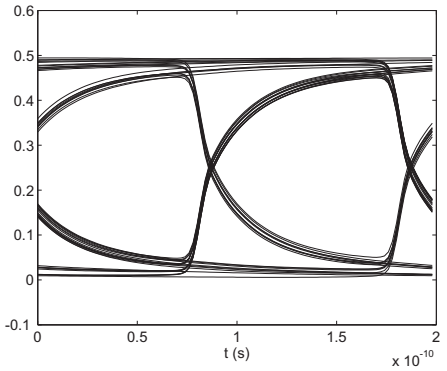
To visualise the influence of an embedded chip on tracks running on top, an eye diagram has been generated for three different configurations and a bit rate of 10 Gbps. The 10 % to 90 % rise time of the input signal is 8 ps and a digital *1* corresponds to a voltage of 500 mV. For the first configuration the width of the microstrip lines without chip is calculated to produce a matched 50 Ω line ($w = 185\,\mu m$ and $t = 20\,\mu m$). The same width is also used for the multilayer microstrip above the chip. The second setup is identical to the first, except for the width of the multilayer microstrip, which is reduced to match 50 Ω ($w = 125\,\mu m$ for $\sigma_{Si} = 10\,S/m$). To investigate the influence of the frequency dependence of the RLGC parameters, a third eye diagram is simulated using $\sigma_{Si} = 0.1\,S/m$. This strongly reduces the frequency dependence and the loss at high frequencies. All sections are still matched to 50 Ω, which requires a slight adaptation for width of the multilayer microstrip ($w = 130\,\mu m$ for $\sigma_{Si} = 0.1\,S/m$). As a reference, the eye diagram for a 30 mm long microstrip without embedded chip is generated as well.

Figure 5.14 shows the eye diagram for the four different setups. The reference case (Figure 5.14(a)) reveals a typical eye diagram for a short board interconnect, with a large eye opening and a slight increase in rise time caused by the attenuation of the highest frequencies. Note that the knee frequency, which is a crude estimate of the highest frequency content of a digital signal [32], is 62.5 GHz for the 10 Gbps signal with a 10 % to 90 % rise time of 8 ps. When the same trace running over an embedded chip is considered (Figure 5.14(b)), the eye starts to close and the rise time of the signal is severely degraded. Because of the short length of the multilayer microstrip, the performance is still acceptable for many digital applications. To determine the influence of the impedance mismatch between the board and the chip, the width of the multilayer microstrip is adapted to produce an impedance of 50 Ω. Due to the

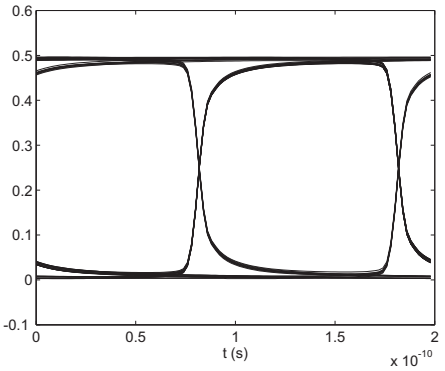


(a) Without chip

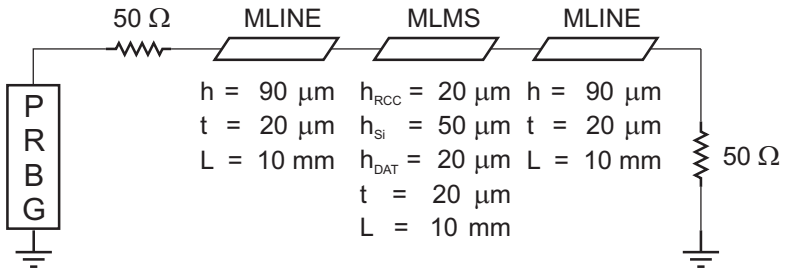
(b) Matched to board



(c) Matched to chip



(d) Reduced conductivity



(e) Configuration for the eye diagram simulation

Figure 5.14: Eye diagram for different configurations of a board interconnect running over an embedded die

strong frequency dependence of the characteristic impedance of the multilayer microstrip, it is not possible to ensure a good match for the entire frequency range. However, above 1 GHz, the reflection coefficient remains smaller than 0.1. The resulting eye diagram is shown in Figure 5.14(c). The eye opening is slightly improved, but the rise time remains almost unaffected. This leads to the conclusion that the main cause of the rise time degradation is the dispersive nature of the characteristic impedance and the loss. To corroborate this conclusion, a final eye diagram is generated for a chip with a reduced conductivity (0.1 S/m instead of 10 S/m). The rise time improves dramatically, even in such a way that it is difficult to see the difference with the setup without embedded chip.

Table 5.3: Summary of the eye diagram timing parameters. t_r represent the 10 % to 90 % rise time, t_{OPEN} the horizontal eye opening (eye width) and V_{OPEN} the vertical eye opening (eye height)

	t_r (ps)	t_{OPEN} (ps)	V_{OPEN} (mV)
Without chip	12	99.83	459.0
Matched to board	118	96.10	333.2
Matched to chip	82	97.15	357.5
$\sigma_{Si} = 0.1\,\mathrm{S/m}$	19	99.79	459.5
$\sigma_{Si} = 100\,\mathrm{S/m}$	56	98.49	431.8
$\sigma_{Si} = 1000\,\mathrm{S/m}$	45	98.99	447.2

A summary of the timing parameters derived from the eye diagrams is given in Table 5.3. The opening of the eye, both in horizontal (t_{OPEN}) and vertical (V_{OPEN}) direction, is still wide enough for digital communication at 10 Gbps. Only the degradation of the rise time can be of some concern, but a part of the voltage budget can be sacrificed to compensate for this. The rise time for the line width matched to the board is even longer than the length of one bit (100 ps). Because of the high reflections for the part of the trace above the chip, the signal takes a very long time to reach 90 % of the voltage swing. Comparing the 20 % to 80 % rise time with the case matched to chip reveals a smaller difference (40 ps versus 42 ps). The eye width gives an indication of the jitter introduced by the interconnection. The jitter increases from 0.16 ps without embedded chip to almost 4 ps for the setup matched to the board. However, this remains insignificant compared to the bit length. Two additional cases are included in the table. Both use a high conductive silicon substrate ($\sigma_{Si} = 100\,\mathrm{S/m}$ and $\sigma_{Si} = 1000\,\mathrm{S/m}$) and the width of the multilayer microstrip is changed to 75 µm to keep the impedance at 50 Ω. The interesting aspect of these configurations is that, due to the slow-wave behaviour, the characteristic impedance remains reasonably constant with frequency, although the loss still shows a strong frequency dependence up to very high values at high frequen-

cies (28.57 dB/cm and 44.34 dB/cm at 62.5 GHz respectively). The reduced frequency dependency of the characteristic impedance significantly lowers the rise time, which is also the case for the low conductive substrate.

5.3.3 Chip metallization

The proposed model assumes that there are no additional conducting surfaces in between the material layers. This is of course not the case for real-world chips. Modern integrated circuits use multiple metal layers of various thickness (e.g. 0.14 µm to 7 µm for Intels 45 nm process generation). Lower layers are used for interconnecting transistors and subregions of the chip, while the upper layers are used for power distribution and connections to the package. These power distribution layers are placed orthogonal to the preceding layer to maximize the capacitive coupling and use thicker traces to transport higher currents. Additionally, embedded chips often require redistribution layers to adapt the pitch and placement of the bond pads to the requirements of the embedding process. All these metal layers shield the influence of the silicon substrate, acting as a virtual ground layer for the microstrip.

The presence of additional conducting structures in between the signal trace and the ground plane of a microstrip has a diverse effect on the propagation behaviour. The total capacitance will increase due to the surface charges induced on the inserted metal. When the conducting structure is grounded, there is no more potential difference between the structure and the underlying ground layer. As a result, the increase in total capacitance is even larger. The time-variant magnetic field will induce eddy currents in the metal structures according to Lenz's law. At moderate frequencies (up to a few gigahertz), these currents are negligible and the effect on the inductance is minimal. When the frequency increases, the magnetic field generated by these eddy currents becomes stronger and reduces the total stored magnetic energy and hence, the inductance starts to decrease. When grounded metal structures run parallel to the microstrip line, the inductance will also be reduced at lower frequencies, since the return current flows closer to the signal trace. The exact distribution of the return current is determined by the path of the lowest impedance. At low frequencies (megahertz range), the resistive part of the return path impedance will be larger than the reactance (ωL) and thus the current will follow the path of the lowest resistance. As frequency increases, the reactance becomes dominant and the return current will try to minimize the loop inductance [88].

Investigations in literature to determine the influence of these patterned metal layers to signals running on adjacent layers, reveal that the presence of orthogonal wiring extends the slow-wave propagation mode up to higher frequencies, minimizing the frequency dependency of the capacitance [89, 90, 91]. Since the orthogonal wires inhibit longitudinal current flow, the inductance is

not affected when the orthogonal lines are not too wide and at moderate frequencies. Conductors running parallel to the signal trace, on the same layer or on the second lower layer, reduce the inductance by bringing the return current closer to the signal trace. Most of these papers describe the propagation behaviour of a low loss slow-wave transmission line, consisting of a microstrip or coplanar waveguide above an orthogonal gridded shield. While these dedicated lines demonstrate the influence of a patterned ground plane above the silicon substrate, they do not take into account the multiple interconnect layers with different orientations. Kleveland et al. [92] however, use a more realistic test structure with global and local power grids, randomly placed underneath the coplanar waveguide. The paper confirms the impact of parallel lines in underlying layers on the line inductance. An interesting observation is made by Quéré et al. [93], who found that for certain resonant frequencies, the signal propagating on a line above an orthogonal grid is strongly attenuated. A correct prediction if this is also the case for microstrips running over embedded chips is difficult to make without further investigations.

The upper IC interconnect layers are used for power distribution and can be assumed to be connect to ground (Since voltage supply lines are decoupled, they are equivalent to ground at high frequencies). The metal thickness and the pitch of the lines are generally around 1 µm, with a total thickness of the interconnect layers in the order of a few micrometer. These layers will thus increase the capacitance and reduce the inductance of the microstrip running over the embedded chip. The capacitance will remain constant with frequency, but the inductance will show a frequency dependency caused by the finite thickness of the metal layers. According to [94], although based on a solid thin-film ground plane, the total thickness needs to be at least two to three times the skin depth to prevent the magnetic field from penetrating through the layers (which corresponds to $f > 4\,\mathrm{GHz}$ for the dimensions mentioned above).

The influence of lines and pads on the redistribution layers (RDL) is harder to predict since these layers are typically less dense and cannot be assumed to be connected to ground. The purpose of the redistribution layer is mainly to fan out the interconnections to the chip in order to make the pitch and the size of the pads compatible with the chip embedding process. As explained in chapter 2, each pad on the redistribution layer is connected to a trace on the board using a microvia. The annular ring of the microvias on the board in combination with the traces connected to these pads, consume most of the board space above the chip, making it unlikely that additional high-frequency traces would be routed across the chip. High-frequency connections *to* the chip can run over the embedded chip for a certain distance, but since the height of the RCC is usually smaller than the spacing between the line and the RDL pads, the influence of these pads is expected to be minimal. Additional routing on the redistribution layer can however still disturb traces on the board. It

is therefore advised to place critical RF signal pads close to the edge of the chip. When the redistribution layer merely consists of enlarged pads without additional routing, the influence of the RDL to signals on top is less pronounced.

The actual behaviour of these intermediate metal layers is difficult to quantify, since it is highly dependent on the density of the routing and the thickness of the metal layers. When the layers are less dense, the influence of the substrate will not be completely shielded, causing the capacitance to show a similar frequency-dependent behaviour as without metal layers. The inductance of the microstrip is determined by the distance between the signal current and the return current and thus dependent on the return current distribution. Modelling these virtual grounds is not straight-forward, because of the complex geometry that needs to be taken into account. The combination of orthogonal and parallel lines requires a three dimensional simulation which needs to take into account the correct return current distributions at every frequency point. Measurements would require dedicated test structures that correctly mimic the real world implementation, but still allow the extraction of general conclusions. A similar approach as used to verify the multilayer microstrip model with long chips to extract the propagation constant is expected to give interesting results about the propagation behaviour, although this may not really reflect the practical implementation.

In an attempt to verify the influence of metal interconnects at the surface of an embedded chip, a simplified two-dimensional quasi-static simulation is performed. The per-unit-length capacitance of a multilayer microstrip is determined for three different configurations: no metal structures at the silicon surface, a thin ground plane on the silicon surface, and a grid of 1 µm lines and spacings, parallel to the signal conductor on the board. The latter geometry was implemented with infinitely thin conductors and with aluminium conductors of 1 µm thick. The simulation results (Figure 5.15) confirm that the presence of additional metal structures increases the total capacitance. When these structures are left floating, the influence of the semiconducting substrate is still visible, even for the case of the solid ground plane. The potential of the metal is determined by the potential of the silicon, which is lower in the slow-wave region than for the dielectric mode [4]. The slow-wave mode for the floating metal structures is extended to higher frequencies, as can be seen from the comparison to the multilayer microstrip with increased silicon conductivity. Connecting the metal structures to ground, shorts the potential of the silicon and thus removes the influence of the semiconducting substrate. There is no difference between the grounded mesh or the solid plane connected to ground (not shown in Figure 5.15). The capacitance for the thick lines is higher, since

[4] The ground plane at the silicon surface can be seen as the upper plate of a parallel-plate capacitor with a conducting and a non-conducting layer. The potential is thus dependent on the frequency and the conductivity of the silicon.

the distance to the signal conductor is smaller.

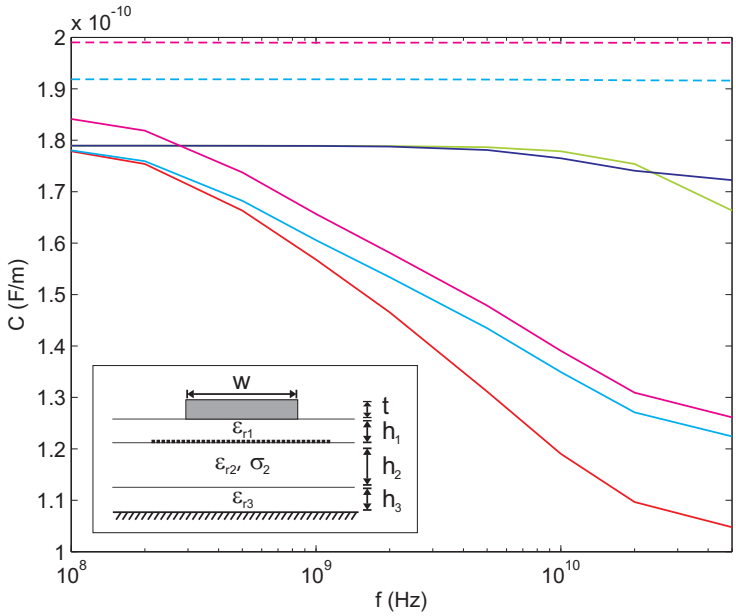


Figure 5.15: Simulated capacitance for different configurations of chip metallization. ($w_{board} = 90\,\mu m$, $t_{board} = 17\,\mu m$, $w_{chip} = 1\,\mu m$, $t_{chip} = 1\,\mu m$, $h_1 = 20\,\mu m$, $h_2 = 50\,\mu m$, $h_3 = 20\,\mu m$, $\epsilon_{r1} = 3.5$, $\tan\delta_{r1} = 0.02$, $\epsilon_{r2} = 12.1$, $\sigma_2 = 10\,S/m$, $\epsilon_{r3} = 3$)
(——) No metal; (——) Solid ground (floating); (——) No metal ($\sigma_2 = 1000\,S/m$); (——) Thin mesh (floating); (——) Thick mesh (floating); (- - - -) Thin mesh (grounded); (- - - -) Thick mesh (grounded)

It is important to note that the proposed model including the influence of the silicon substrate is still valid for several practical implementations. For example, when a trace is running underneath the chip, close to the bare backside of the chip, there are no intermediate metal layers to shield the silicon substrate. In the case of a pad-limited IC design, certain areas of the chip are mainly bare silicon.

5.4 Additional comments

In this section, a number of shortcomings of the proposed model are addressed. A conscious choice was made for a simple, but accurate model that can easily be applied using existing closed-form microstrip design formulas. These formulas are still widely used by PCB designers to determine, for example, the impedance

of high-speed interconnections. A modelling approach that remains compatible with current PCB design tools can catalyse the acceptance of chip embedding as a packaging technology. As a compromise, this method does not yield the highest accuracy.

The model presented in this research is based on established techniques that are adapted to correctly predict the behaviour of tracks running near components embedded in a printed circuit board. Due to the complex geometry and the use of advanced materials in an unusual stack up, the characterization of these board interconnects cannot be performed using current RF *circuit* simulators. The integration of 3D electromagnetic solvers into the design flow is starting to emerge. Their computational cost is, however, still too heavy for sizeable design purposes and for the integration in circuit simulators, where large and complex layouts need to be evaluated quickly. A number of fast, two-dimensional EM solvers are becoming more and more popular to extract circuit parameters for planar waveguide geometries (e.g. Ansoft Maxwell 2D Extractor or Polar Instruments PCB Transmission Line Field Solver). Especially PCB manufacturers welcome the ability to input the complete board stack-up as a starting point for the controlled impedance evaluation. A drawback of these solvers is that they fail to take into account the losses in both conducting and semiconducting layers over a broad frequency range. Combining the effective dielectric constant and the effective height, calculated by the proposed model, with these kind of solvers, results in a powerful and accurate tool for controlled impedance of traces running near embedded chips.

A limitation of the proposed model is that it is currently restricted to single-ended microstrips. Coplanar waveguides and coupled microstrips on multilayer substrates were successfully modelled in the past using the complex image approach [73] and the single-layer reduction [95, 96]. To use the variational expression of Yamashita [69], the latter required suitable charge distribution functions for the odd and even mode separately. A thorough investigation of the accuracy of these approximations to predict the behaviour of coplanar waveguides and coupled microstrips running near embedded components would be needed.

The technology for chip embedding that is used for this research is the embedding of thin chips in the build-up layers for the PCB. This approach is chosen since it is available in-house and quite some experience was gained during the development of the technology. A minus point is that this technology is not the most likely to be used in the industry at this point, and consequently is not as robust as other approaches. Since the material stack for other embedding techniques is similar, the results can be applied there as well. As an example, the influence of thicker silicon, used for chips embedded in the core layers, has been studied and is predicted well by the model.

The design and manufacturing of a dedicated measurement test vehicle

required several iterations over a significant period of time. The issues encountered during manufacturing show that the in-house technology for embedding chips in printed circuit boards is not completely mature yet; however, the specific nature of the test vehicles with the large monolithic dies is exceptional. In the end, the test vehicle made it possible to extract the propagation constant of traces running on top of embedded dies in a reliable way.

Chapter 6

Conclusion

Don't waste your life engineering the details of each and every via
Howard Johnson

The aim of this doctoral research is the high-frequency characterization of active chips embedded in printed circuit boards. To evaluate the merit of this endeavour, a number of questions have to be answered. Does chip embedding in printed circuit boards have a market potential as advanced packaging technology? Is this packaging concept a suitable choice for high-frequency applications? Do the results presented in this research aid the designer in implementing this new technology to its full potential?

In general, advanced packaging concepts are gaining acceptance in the industry. Fan-in WL-CSP, for example, is increasingly used in hand-held applications for its reduced footprint and package height. The volume production of mobile devices has led to a significant cost reduction for wafer level packaging and as a result, this technology is appearing in automotive, medical, computing, and digital photography applications. According to Yole Développement, WL-CSP can reach a market share of 15 % to 20 % by 2020. Chip embedding can benefit from this evolution, as the die preparation steps needed for embedding are similar to the wafer level packaging process. For small dies with low I/O count, embedding can further reduce the packaging cost through the large-scale production typical for PCB manufacturing, provided that the yield can be controlled.

In the area of 3D packaging, a lot of research effort is put into 3D IC technologies using through silicon vias (TSV) to interconnect stacked dies. In combination with silicon interposers, this approach makes it possible to integrate passive devices and is compatible with fine-pitch flip-chip technology. The

widespread adoption of the TSV technology is hindered by the high manufacturing cost and supply chain issues. Stacking of embedded chips is a very versatile and flexible solution which can be used for realizing complex 3D system-in-package modules. With further technology improvements such as higher yield, lower profile and finer pitch, embedded components may seriously compete in the fast-growing 3D packaging market.

A significant number of PCB manufacturers are ramping up their embedded component facilities: Casio (Tokyo, Japan), Ibiden (Ogaki, Japan), AT&S (Vienna, Austria), Imbera/Daeduck (Espoo, Finland/Kyonggi-Do, Korea) and Taiyo Yuden (Tokyo, Japan). The added value of boards with embedded components opens up new markets for these companies, offering higher margins compared to traditional printed circuit board manufacturing. At this moment, however, it is too early to tell if this technology will capture a relatively important portion of the advanced packaging business. Continuing research on both technology aspects as application specific demands are needed to reach the maturity level required for a reliable packaging technology.

Although the technology process itself is quite mature, the practical implementation needs to be carefully analysed, depending on the specific application. For example, applying a redistribution layer to a large die can impose manufacturing restrictions on the thickness of the silicon, making it very difficult to maintain a controlled impedance over a broad frequency range. Not all of these application-dependent restrictions are known, impeding the assessment of chip embedding as a technology for high frequencies. To a larger extend, the high-frequency modelling is hindered as well, since the material stack and the overall geometry are prone to changes. Another consequence of introducing a new technology is that manufacturing tolerances are still quite large and thus have to be taken into account during the modelling.

Embedding chips in printed circuit boards has a number of high-frequency advantages. The reduced interconnection length between chip and board and the impedance control along the entire signal path are the most important benefits. The potential to easily shield the embedded component from its surroundings is also an advantage. Due to the very small distance between the interconnects on the chip and the routing on the board, interference from chip to board and detuning of chip interconnects are possible challenges.

When evaluating the high-frequency aspects of embedding chips in printed circuit boards, the actual implementation of the technology is important. If the final product will be used as a package, the interconnection between the chip and the package substrate will be the most important aspect. Intelligent placement and routing of the redistribution layer will minimize the influence of the semiconducting silicon. When the embedded chip package and the integrated circuit can be co-designed, the high-frequency performance of the interconnection is believed to be at least on par with dedicated flip-chip implementations.

The system-in-board approach combines multiple embedded dies with passive and active components. Here, interference between chip and board and the propagation behaviour of tracks running on top of embedded chips become important.

In this research, a model is developed to predict the propagation behaviour of traces running near embedded components. Despite the low amount of measurement samples, some general conclusions concerning the accuracy of the model can be drawn. The accuracy depends to a large extend on the accuracy of the input parameters, more precisely the geometry and the material parameters. For dedicated materials, the parameters can often not be verified since these materials are not available in bare format. The sensitivity analysis revealed that the most critical material is the resin above the chip, for which the dielectric constant and the loss tangent can be determined quite accurately.

The model was verified using the propagation constant extraction and S-parameter measurements of lines running over a chip, with acceptable results. The model is accurate to within a few percent for the effective dielectric constant, but shows a larger error for the predicted total loss. The loss is more sensitive to the input parameters and thus harder to model. However, the observed accuracy of ± 10 % is sufficient for signal integrity investigations on large and complex cirucits, as can be seen from the eye diagram analysis.

Further investigations into the influence of the chip metallization will complete the modelling of printed circuit board traces running on top of embedded components. Setting up an accurate simulation environment and designing dedicated measurement samples for this, are not trivial. Along with a more extended study of interference between signals on the chip and the board, this will lead to dedicated design rules for the implementation of embedded components in high-frequency systems.

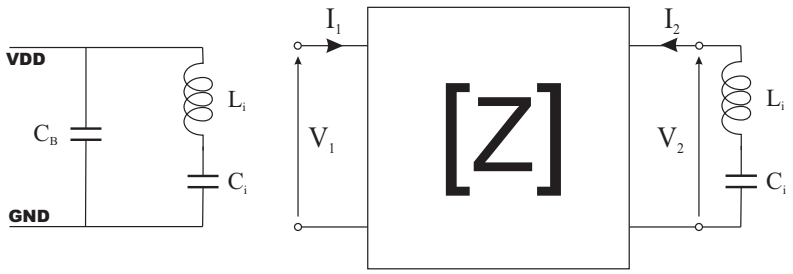
Appendix A

Power integrity study for embedded passive components

The power delivery network (PDN) of a system is usually comprised of a voltage regulator module (VRM) that generates the supply voltage V_{DD}, connected to power planes that distribute this voltage across the board. To prevent voltage drops when the current draw of one of the components suddenly changes, decoupling capacitors are added, effectively lowering the impedance of the power delivery network. This voltage drop is commonly referred to as *ground bounce*. By dividing the tolerated voltage ripple by the maximum (transient) current, the target impedance for the PDN can be calculated. The actual impedance of the power delivery network, Z_{PDN}, has to be smaller than this target impedance over the complete frequency content of the transient currents. Slow transient currents can be handled by the VRM, however faster transients require global or local decoupling capacitance in combination with high capacitance power planes [97].

The performance of the decoupling capacitors is degraded by the parasitic inductance (and resistance) in series with the capacitor. This inductance is due to the effective series inductance (ESL) of the component itself in combination with the trace induction of the connection between the capacitor and the power planes. The aim of this power integrity study is to verify if embedding the decoupling capacitors in between the power planes can effectively reduce this parasitic inductance and result in a better decoupling behaviour.

At low frequencies (below 100 MHz), the power delivery network can be modelled using a lumped component network consisting of the bulk capacitance



(a) (b)

Figure A.1: Lumped element model (a) and distributed impedance model (b) for the power planes in combination with multiple decoupling capacitors, represented by parallel branches L_i, C_i

of the power planes in parallel with several LC networks for each decoupling capacitor (Figure A.1(a)). The resulting impedance shows a series resonance for each parallel branch at

$$f_{res} = \frac{1}{2\pi\sqrt{L_i C_i}} \tag{A.1}$$

and a parallel resonance in combination with the interplane capacitance at

$$f_{res} = \frac{1}{2\pi\sqrt{L_i \frac{C_i C_B}{C_i + C_B}}}. \tag{A.2}$$

When the frequency rises, the power planes start to show a distributed behaviour (Figure A.1(b)), resulting in several board resonances for wave lengths matching the power plane dimensions. For a power plane pair of size w x w, the first board resonance frequency is

$$f_{01} = f_{10} = \frac{c}{2w}\frac{1}{\sqrt{\epsilon_r}}. \tag{A.3}$$

Figure A.2 compares the magnitude of the impedance of the bare board (5 cm by 5 cm) to the situation with an added decoupling capacitance of 1 nF. Up to the first resonance, both configurations act as a capacitive load. The bare board has a capacitance of 0.05^2 3.9 $\epsilon_0/220\,\mu\text{m} = 392.4\,\text{pF}$ and a resonance frequency of about 370 MHz. The added decoupling capacitance reduces the power plane impedance at low frequencies. The first resonance occurs at 100 MHz, caused by the parasitic inductance of the connection to the power

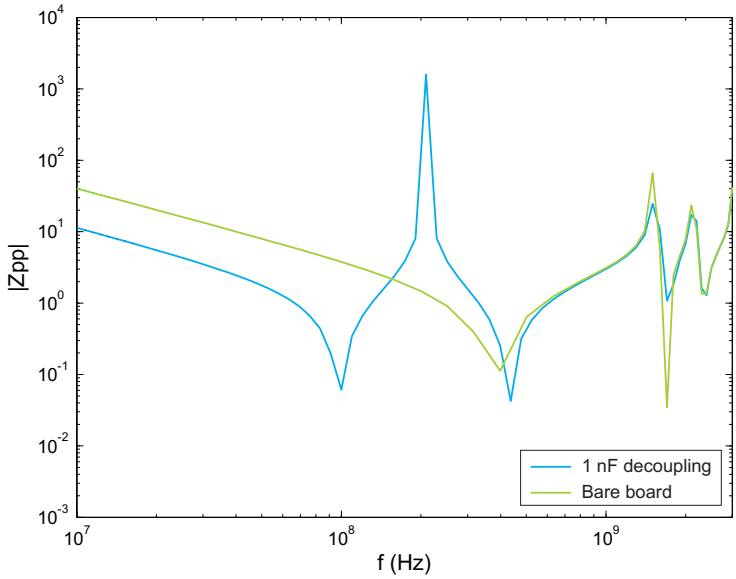


Figure A.2: Simulation results for a 5 cm by 5 cm power plane pair with a 220 µm thick dielectric in between ($\epsilon_r = 3.9$). The green line shows the bare board, the blue line shows the same board with an ideal decoupling capacitance of 1 nF

planes in combination with the 1 nF capacitance. The following peak (anti-resonance) at about 200 MHz is caused by the bulk capacitance in parallel with the LC circuit of the decoupling capacitance. Above 1 GHz, the distributed behaviour of the planes becomes visible with a first board resonance at around 1.5 GHz.

The distributed impedance between two locations ("ports") on the board can be calculated using a Green's function of the 2D-Helmholtz equation [98]:

$$Z_{ij}(\omega) = j\omega\mu\frac{h}{w^2}\sum_{n=0}^{\infty}\sum_{m=0}^{\infty}\frac{\epsilon_n^2\epsilon_m^2}{k_{mn}^2 - k^2}\, f(x_i, y_i)\, f(x_j, y_j) \tag{A.4}$$

where

$$f(x_i, y_i) = \cos\left(\frac{m\pi x_i}{w}\right)\mathrm{sinc}\left(\frac{m\pi t_{x_i}}{2w}\right)\cos\left(\frac{n\pi y_i}{w}\right)\mathrm{sinc}\left(\frac{n\pi t_{y_i}}{2w}\right) \tag{A.5}$$

The parameters are explained in table A.1.

This analytical expression provides the complete two-port impedance matrix with Z_{ii} being the self-impedance at each port and Z_{ij} the transfer-impedance between ports. Consider the component drawing current at one

Table A.1: Parameters for the calculation of the distributed impedance

w	Width of the power plane
h	Spacing between the planes
ϵ_n, ϵ_m	1 for $m, n = 0$, and $\sqrt{2}$ otherwise
k	Propagation constant
k_{mn}	Wave number
x_i, y_i	Coordinate of port i
t_{x_i}, t_{y_i}	Dimensions of port i

port and the decoupling capacitor at the second port. With Z_L being the equivalent impedance of the parasitic inductance and the capacitance of the decoupling capacitor, the input impedance seen by the component becomes

$$Z_{in} = Z_{PDN} = Z_{11} - \frac{Z_{21}Z_{12}}{Z_L Z_{22}}. \tag{A.6}$$

This formula can be used to determine the parasitic inductance of the decoupling capacitance from measurements or simulations.

The extraction of the input impedance from the S-parameters requires a 2-port measurement. The reason for this is that due to the low values of the power plane impedance, the reflection coefficient S_{11} is close to 1 and the dynamic range of the VNA is limited at these values. The solution is to use a 2-port measurement and extract the power plane impedance from S_{21}. With a port impedance of 50 Ω, the relation between Z_{PDN} and S_{21} becomes

$$Z_{PDN} = 25\frac{S_{21}}{1 - S_{21}}. \tag{A.7}$$

This approach is also applied to the simulations. To limit the simulation time, the comparison between the model and the simulation was performed for a 5 cm by 5 cm power plane pair, with the probe structure close to the corner of the plane.

The first simulation is run to calculate the impedance of the bare board (Z_{11}). As can be seen from formula (A.4), the self-impedance Z_{11} is dependent on the dimensions of the power plane pair (5 cm by 5 cm by 220 µm), the location of the port ($2\,\mathrm{x}\,10^{-3}$; $2\,\mathrm{x}\,10^{-3}$) and the size of the port (500 µm by 500 µm). The calculated impedance perfectly fits the result from the simulation. The second step is to add the port structure for the surface-mount (SMD) capacitor. To mimic a four layer board, two plated through-hole (PTH) vias to the outer layers are added and a circuit port is drawn between the pads on the top layer (Figure A.4(b)). The simulation is also performed with an embedded decoupling capacitor, which requires only one PTH to connect the capacitor

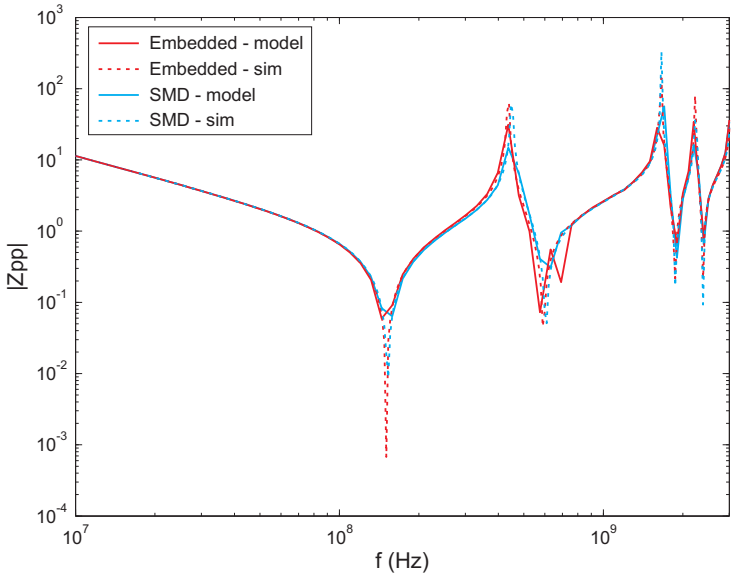
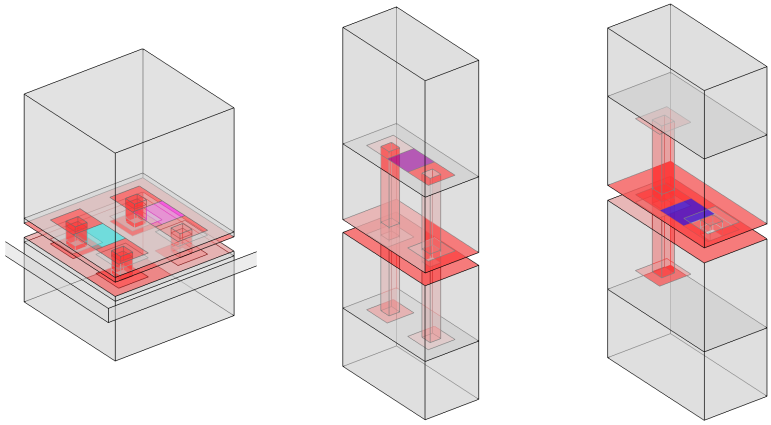


Figure A.3: Simulation and modelling results for a 5 cm by 5 cm power plane pair with a 220 µm thick dielectric in between ($\epsilon_r = 3.9$). The excitation and measurement port are near the origin ($2\,\mathrm{x}\,10^{-3}$; $2\,\mathrm{x}\,10^{-3}$), while the decoupling capacitor is located at (0.04 ; 0.04)

to the power planes (Figure A.4(c)). In both cases, the decoupling capacitor was an ideal 1 nF capacitance, so the parasitic inductance was only due to the interconnect method. Figure A.3 shows the results of these simulations, with near perfect correspondence between the simulations and the model.

The difference between the parasitic inductance for the embedded capacitor and the SMD version is very small (0.24 nH versus 0.27 nH). This is due to the low layer count of the board and thus the short length of the via. To get a more realistic comparison, the number of layers of the surrounding board is increased. The new simulated build-up consists of a core with 12 layers of 200 µm (except the power plane pair separation which was kept at 220 µm) with three build-up layers of 100 µm on each side, resulting in an 18-layer board, 2.82 mm thick. The power plane pair was situated in the middle of the core (layer 9 and 10). Figure A.4 gives a detailed view of the implementation of the excitation port and the decoupling capacitors.

Figure A.5 compares the results for the 4-layer board to the 18-layer board, both with a 1 nF decoupling capacitor. The resonance for the embedded capacitor does not change significantly with the increased layer count. The case with the surface-mount capacitor however, shows a large increase in parasitic



(a) (b) (c)

Figure A.4: Detailed view of the probe structure (two-port excitation, a), the interconnection structure for the SMD capacitor (b) and the embedded capacitor (c). Metal structures are indicated in red, port 1 is cyan, port 2 is magenta, the circuit port for the SMD is purple and the circuit port for the embedded capacitor is blue

inductance due to the long vias through the board. Here the advantage of embedding the component in between the power planes is very clear. Using buried vias would further increase this advantage.

This power integrity study is by no means a complete characterisation of the use of embedded passive components for power decoupling. The model should be expanded to a large numbers of decoupling capacitors and compared to measurements of dedicated test vehicles. However, the advantage of embedding the decoupling capacitors in between the power planes of complex board is adequately demonstrated.

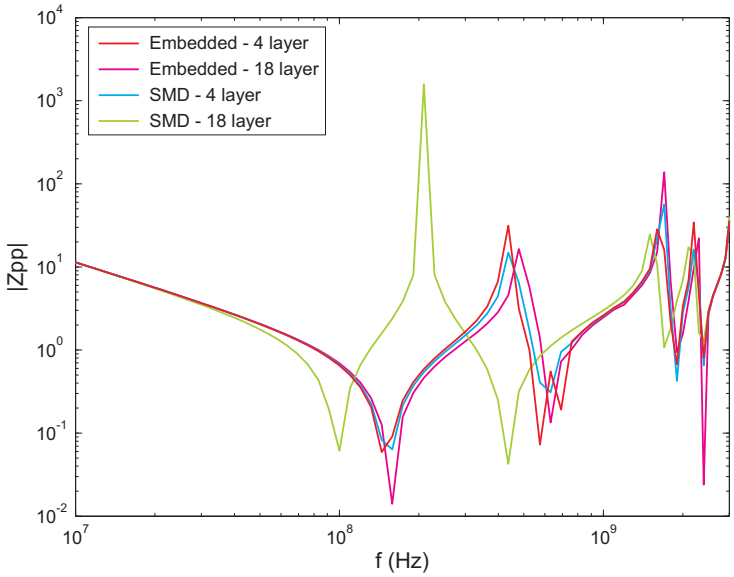


Figure A.5: Comparison of embedded and surface-mount decoupling capacitors for a 4- and 18-layer board. (5 cm by 5 cm power plane pair with a 220 µm thick dielectric in between ($\epsilon_r = 3.9$))

Appendix B

Design and specifications of the HIDING DIES test vehicles

TV1

TV1 Build-up

Table B.1: Overview of the build-up of TV1

Layer	Type	Material	Thickness (µm)
S1	Conductor	Cu	20
D1	Dielectric	RCC	70
S2	Conductor	Cu	17
D2	Dielectric	FR4	600
S3	Conductor	Cu	17
D3	Dielectric	RCC	70
S4	Conductor	Cu	20

The build-up of the first test vehicle was kept as simple as possible, containing only a single layer of embedded dies. A two-layer core substrate is covered on both sides with a build-up layer, resulting in a four layer board. Table B.1 gives an overview of the build-up of TV1. The test chips are embedded in the top build-up layer D1, and the chip thickness is 50 µm. This was the lowest thickness that could be achieved in a reliable way and on a production scale at the beginning of the project. The empty areas on all layers are filled with Cu

to improve the etching results and for better control of the dielectric thickness of the inner layers. TV1.1 contains only microvias between S1 and S2, so there are no connections to the backside of the board. TV1.2 contains PTH from S2 to S3 and microvias from S3 to S4. The PTHs are situated next to the die and are filled with epoxy during lamination.

TV1 Layout rules

Table B.2: Layout rules for TV1

Core	(µm)
Min. Via Hole Diameter	200
Min. Via Land Diameter	500
Min. Outer Layer Track Width	75
Min. Outer Layer Spacing	75
Min. Distance Thermal Hole - Embedded Die	150
Dies	
Min. Pitch	200
Die Bond Adhesive Layer Thickness	20
Build Up Layer	
Microvia-to-core Diameter	100
Microvia-to-core Land Diameter on core	200
Microvia-to-core Land Diameter on top	200
Microvia-to-chip Diameter	50
Microvia-to-chip Land Diameter	150
Track Width	75
Clearance Track to Track	75
Clearance Track to Pad	70
Solder mask	
Solder Mask to Cu Registration	38
Min. Solder Mask Opening	100

The layout rules for TV1 are shown in Table B.2. Most of these rules are common in advanced printed circuit board processing, allowing the manufacturing to focus on the chip embedding.

TV1 Components

Initial technology trials were performed with dummy test chips consisting of only silicon and a daisy chain metallization pattern. These chips allow for an easy verification of the integrity of the interconnects to the chip at a low cost.

Table B.3: Different daisy chain test chips used for TV1

Type	Size	Thickness	I/O pitch	I/O	FPM	dies
IZM21.1	10 x 10 mm^2	50 µm	200 µm	184	16	5
IZM21.2	10 x 10 mm^2	50 µm	300 µm	120	16	7
IZM30.1	5 x 5 mm^2	50 µm	200 µm	84	8	12
IZM30.2	5 x 5 mm^2	50 µm	300 µm	56	8	12
IZM28	2.5 x 2.5 mm^2	50 µm	300 µm	20	0	36

The size of the chip is varied to detect a possible influence on the die bonding accuracy and warpage of the chips. The different daisy chain test chips and their specifications are given in Table B.3. The number of chips used in the design as well as the number of connections and four-point measurement test structures per chip are indicated in the table. All bond pads are 100 µm x 100 µm, with 80 µm x 80 µm passivation opening. The small IZM28 chips are mainly used for testing the resin flow in between the chips. The chips are placed in groups of 9 with distances in between of 1, 2, 3 and 4 mm. The IZM30 test chips are placed in groups of 4 with distances of 1, 2.5 and 4 mm. And finally, the IZM21 chips are placed as a single chip with distances of 1, 2.5 and 4 mm. The high number of chips results in about 20 % of the area of the board covered with silicon.

For thermal management testing a total of 6 thermal test chips are embedded. The thermal test chip is the PST1-02 from Delphi (Figure B.1). This 2.54 x 2.54 mm^2 thermal chip provides resistive heating by driving a current through a doped silicon well between a pair of bus bars. Temperature monitoring can be done with a serial five-diode temperature sense network or using an internal bridge network.

The signals are routed to two board-to-board connectors for easy testing and measurements. These include power and ground for the bridge network, current for resistive heating and connections to the thermal diodes. Ground (pin 30) and S2 (pin 29) from the bridge network, D3 (pin 31) and D4 (pin 32) from the sense network are common for half of the chips. This results in 8 connections per chip and two times 4 common connections, for a total of 56 connections. In addition to the tracks to the connector, pin 9 and pin 10 are connected to two test pads next to the chip. These two pins connect to a track running the circumference of the thermal test chip and serve as a quick test for the integrity of the chip.

To characterize the different possibilities of heat transfer, three types of thermal implementations are used. The first implementation uses minimal interconnections to the chip, resulting in a minimum amount of Cu above the chip (Figure B.2). Directly below the chip on layer S2 there is copper,

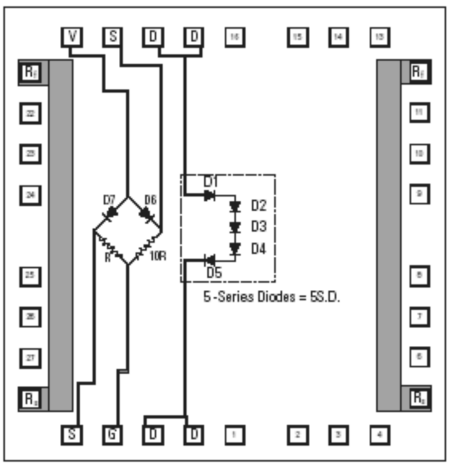


Figure B.1: Delphi PST1-02 Thermal Test Chip

but surrounding that there is a 10 x 10 mm^2 opening in the Cu-fill, thermally insulating the chip from the neighbouring copper planes. This is implemented on all versions of TV1.

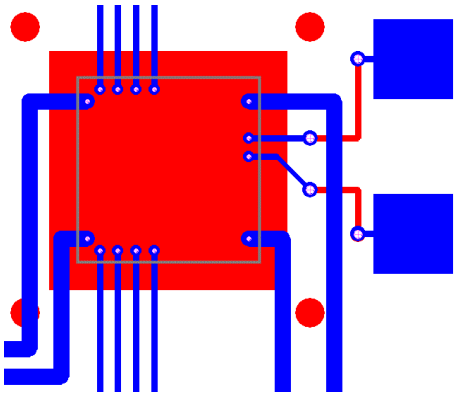


Figure B.2: The first implementation of the thermal test chips: minimal interconnect. Layer S1 is blue, Layer S2 is red and chip outline is grey

For the second implementation the remaining pads are connected to a Cu-area on layer S1 above the thermal chip (Figure B.3). The copper layout on layer S2 is the same as for the first implementation. This is also available on all versions of TV1. The last implementation is the same as the second, but with the Cu-fill connected to layer S2 using microvias (Figure B.4). For TV1.2,

this layer is then connected with thermal PTH to the back side of the core (S3) and further down with microvias to S4. The Cu-fill below the chip on layer S2 extends as far as these thermal PTHs.

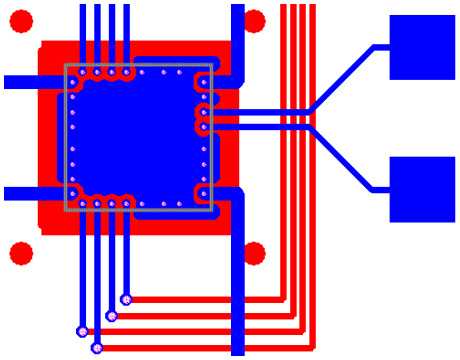


Figure B.3: The second implementation of the thermal test chips: Cu-fill above the chip

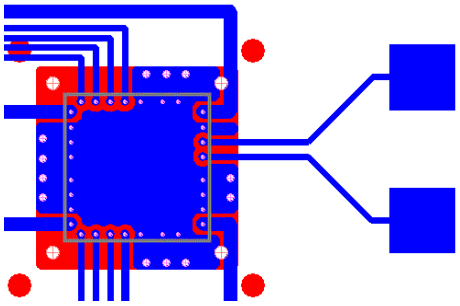


Figure B.4: The third implementation of the thermal test chips (TV1.2): Cu-fill connected to lower layers. Again layer S1 is blue, S2 is red and the chip outline is grey. The holes are drawn in pink

To have a functional die available in the test vehicle, high-frequency transistors are embedded. A single transistor has dimensions of 0.28 x 0.28 mm^2. A 2 x 2 transistor matrix is sawn from the wafer in order not to run into problems handling too small dies. Only one of the four transistors is connected to the test pads, see Figure B.5. A total of four connected transistors are available in the design.

For easy connection to external test systems the connections from the thermal test chips and some of the daisy chains and insulation test patterns are routed to a board-to-board connector. To supply enough connections two 0.8 mm pitch, 60 pin SMD connectors from AMP are positioned on the top

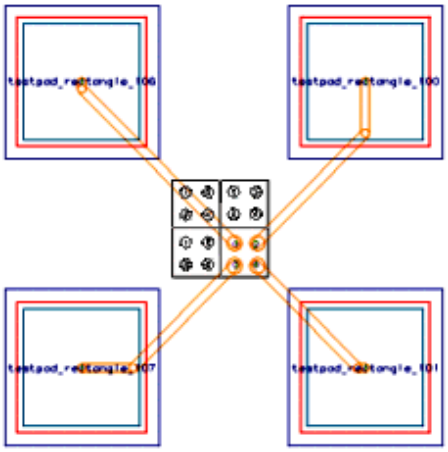


Figure B.5: The transistor array as implemented on TV1. Only 1 of the 4 transistors per chips is connected to the test pads. This structure is implemented 4 times on the test vehicle

layer of the board.

TV1 Test structures

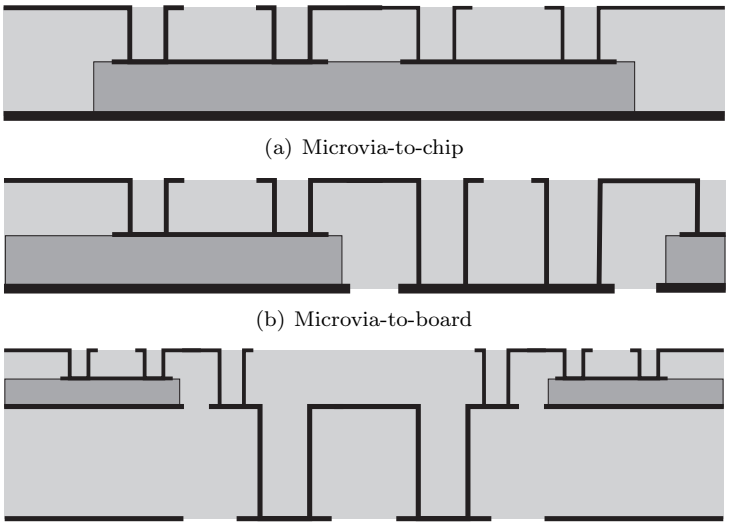
A straight-forward way to verify the integrity of the interconnections to the chips or to detect cracks in the silicon is to incorporate the test chips into a daisy chain running on and off the chip. Three different types of daisy chains are implemented: microvia-to-chip, microvia-to-board and microvia-with-PTH. The necessary test pads are provided for quick manual measurements. Some of the chains are routed to the connector.

Microvia-to-chip The daisy chain consists of multiple vias between S1 and the traces on the surface of the chip. The pitch depends on the pitch of the test chips. Via hole diameter is 50 µm in a 150 µm via land. There are a total of 17 of these daisy chains on all versions of TV1. (Figure B.6(a))

Microvia-to-board For reliability testing of connections from chip to board some daisy chaining of via-to-chip and via-to-board is done. These chains continue on the next chip. Besides the pitch, the distance of the microvias to the edge of the chip is also varied. There are 4 of these daisy chains on TV1.1 and 2 on TV1.2. (Figure B.6(b))

Microvia-with-PTH Plated through holes applied for thermal reasons can be used as signal vias as well. For this reason PTH placed close to the

chip are incorporated in a via chain going from one chip to the next. There are 2 of these daisy chains on TV1.2. For TV1.1 these are replaced by microvia-to-board daisy chains. (Figure B.6(c))



(a) Microvia-to-chip

(b) Microvia-to-board

(c) Microvia-with-PTH

Figure B.6: Daisy chain configurations

To be able to bypass broken sub chains and also to keep the functionality of the test vehicle without having to fully populate every board, every sub chain can be shorted by an SMD short. This makes it possible to continue with automated measurements from the connector in these cases. The contact pads of these SMD shorts also function as test pads for manual measurement of the sub chains.

To test the ability of placing SMD components on top of an embedded chip, two SMD chains are incorporated in the design. These can only be measured through manual test pads and are placed above the IZM21 chips.

The IZM21 and IZM30 test chips contain the necessary structures for four-point measurements. These are used to measure the contact resistance of the microvia-to-chip. Spacing of the contacts to accommodate the probe positions for automated probing is 200 µm, with 100 µm probe pads. All FPM structures on the test vehicle are oriented in the same way to allow semi-automatic measurements.

Instead of normal interdigitate comb-pairs, special meander structures are used for measuring both insulation and shorts. These structures can be placed

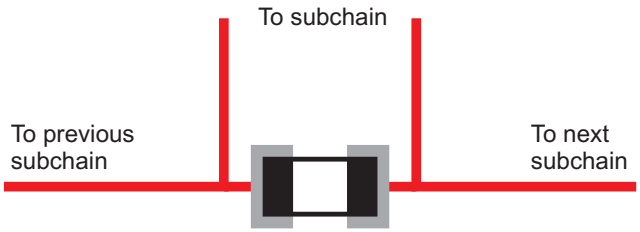


Figure B.7: SMD short for bypassing sub chains

on chip, off the chip and over the edge of a chip to verify if there is any influence of the embedded chip on the process variations. The spacing and width of the tracks are 100 µm/100 µm; 75 µm/75 µm; 50 µm/50 µm; and 40 µm/25 µm. Every insulation test pattern has sufficient test pads to evaluate the structure by hand. The 100 µm and 75 µm structures are connected in series, with the end points routed to the connector.

Four chips in the outer corners of the substrate are reserved for HF measurements. The test structures evaluate the controlled impedance of microstrips running over the embedded dies (two chips) and some via characterization (the other two chips).

The length of the microstrips is 2 cm (Figure B.8). The first strip has a width of 275 µm, resulting in a 50 Ω impedance for the RCC layer (not above the chips). The second and third microstrip have a width of 233 µm and 221 µm, resulting in around 50 Ω for the parts running over the chips, determined using Agilent ADS Momentum. The last two strips are 275 µm wide for the RCC and smaller above the chips: 233 µm and 221 µm. [1]

TV1 Layout

The placement of the different chips and other components, as well as the location of the daisy chains, insulation test patterns and the high-frequency test structures are shown in Figure B.9.

[1] Since the main purpose of the test vehicle is the evaluation of the embedding technology, these test structures were never fully intended to be used for high-frequency characterisation. The synthesis of the geometry was performed at a very early stage, both technology-wise as from a RF modelling point of view, so the details will not be further discussed. However, measurement results are presented in chapter 5.

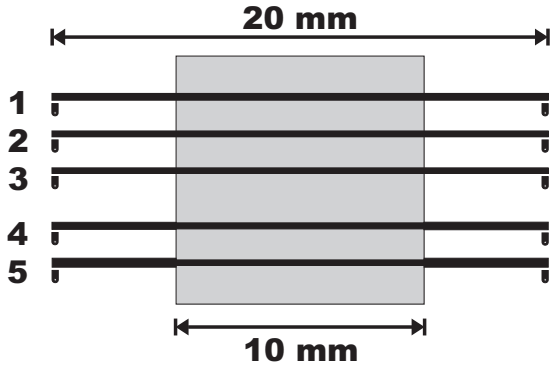


Figure B.8: Layout of the microstrips above the IZM21 test chip. Widths are (from top to bottom): 275 µm, 233 µm, 221 µm, 275 µm + 233 µm and 275 µm + 221 µm

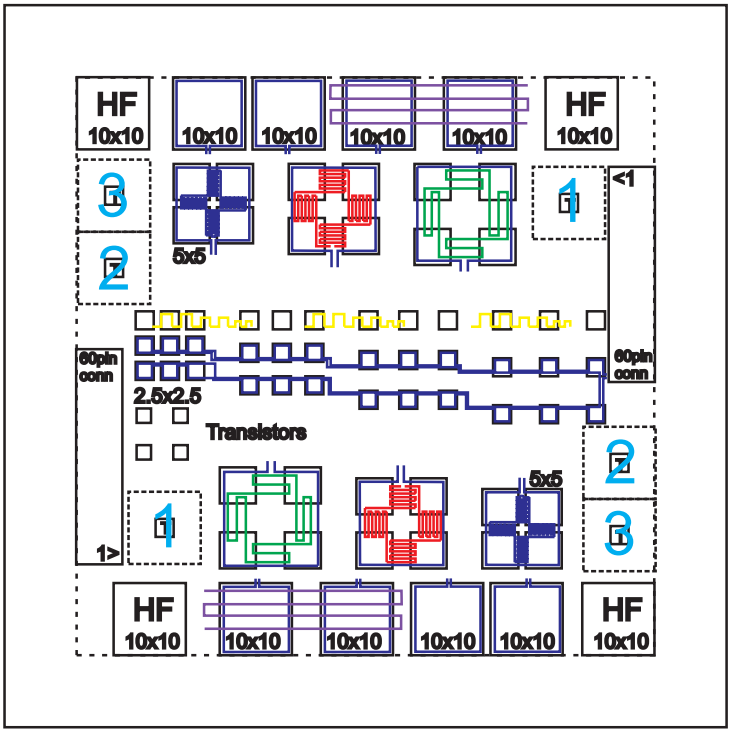


Figure B.9: Location of the different test structures on the TV1 test vehicle: Microvia-to-chip chains (dark blue), Microvia-to-board (red), Microvia-with-PTH (green), Insulation test patterns (yellow), SMD chains (purple), Thermal test chip locations (light blue)

TV2

An important part of any packaging technology is the evaluation of the thermal management of the chips and the thermo-mechanical behaviour of the package. Most of the evaluation is done through thermo-mechanical simulations, but real-world thermal measurements are still needed to verify the simulation results, especially in the case of new technologies. A dedicated thermal test vehicle was designed with a simple layout to make it easier to compare the measurement results to the simulation, which posed a problem for the complex layout on TV1.

TV2 Build-up

Table B.4: Overview of the build-up of TV2

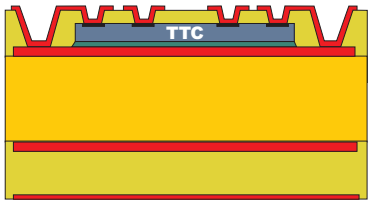
Layer	Type	Material	Thickness (µm)
S1	Conductor	Cu	25
D1	Dielectric	RCC	90
S2	Conductor	Cu	25
D2	Dielectric	FR4	150
S3	Conductor	Cu	25
D3	Dielectric	RCC	90
S4	Conductor	Cu	25

Chips are embedded in the top build-up layer D1. Targeted chip thickness is 50 µm. Experiences from TV1 show a variation in chip thickness of ± 10 µm. To ensure sufficient RCC height above the chip, especially with the low amount of silicon, a thicker RCC of 90 µm was chosen.

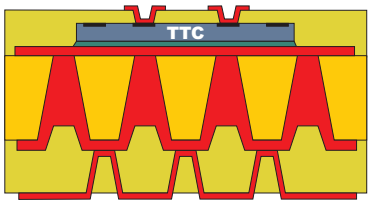
Thermal finite element method simulations, performed by CWM, revealed that the best cooling results are obtained by using a direct thermally conductive path to the outside of the board. Since the vias on the top side are usually reserved for electrical interconnections, dedicated thermal vias from the backside of the chip to the bottom layer of the board are used as thermal path. To be able to test this optimal thermal configuration, there is a need for vias directly underneath the chip. The use of mechanically drilled PTHs would require these holes to be filled and the copper above would need to be smoothed to achieve good die bonding results. An easier solution is to use a thin core and drill the vias from the backside using laser drilling without punching through the copper layer underneath the chip. This leaves the die bonding surface intact and the resulting vias can be filled using extra copper plating.

To evaluate the thermal performance of the embedded dies there are three

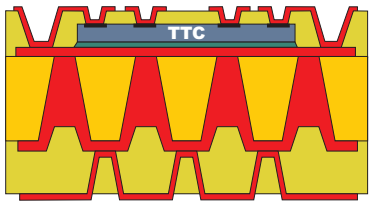
different implementations for the cooling of the thermal test chips. The first implementation (TTC1 - Figure B.10(a)) uses a thermal path upwards only. The copper planes above and below the chip are connected using microvias. There are no vias to the backside of the board. The second implementation (TTC2 - Figure B.10(b)) only has a thermal path to the backside of the board. There is no copper plane above the chip and only the pads required for the thermal measurements are connected. The copper plane under the chip is connected to the backside using vias through the core and microvias in the bottom build-up layer. These vias between S2 and S3 and between S3 and S4 are placed both under as next to the die. The third implementation (TTC3 - Figure B.10(c)) is a combination of the other two implementations as it has both a thermal path upwards and downwards.



(a) TTC1 with thermal path upwards



(b) TTC2 with thermal path downwards



(c) TTC3 with thermal path in both directions

Figure B.10: The three thermal implementations on TV2

Because of the importance to the thermal performance of the embedded chips, also the Cu thickness of plated vias and signal layers are part of the design specifications of TV2. The process of embedding the chips is equal to the standard process flow for embedding active components. However, to retain a flat Cu surface underneath the chip, the via holes through the core are laser drilled from the backside. After drilling, an extended Cu plating process is used to deposit sufficient Cu into the via holes.

TV2 layout rules

The layout rules for the second test vehicles are identical to those of TV1 (see section B).

TV2 components

The thermal test chip is the PST1-02 from Delphi (Figure B.1). This 2.54 x 2.54 mm^2 thermal chip provides resistive heating by driving a current through a doped silicon well between a pair of bus bars. Temperature monitoring can be done with a serial five-diode temperature sense network or using an internal bridge network. The integrity of the chip can be checked using a dedicated track that runs along the perimeter of the die and is connected to pin 9 and 10. These pins are connected to two manual test pads on the board for quick integrity testing.

The operating signals are routed to solder pads, to allow some freedom in the way the boards are connected to the test equipment. The necessary connections are power, ground and sense for the bridge network, current for resistive heating and connections to the thermal diodes. The remaining dummy chip pads are connected to the copper plane above the chip for TTC1 and TTC3.

TV2 layout

To achieve optimal results from the thermal modelling and measurement, the layout and routing is kept as simple as possible. The routing for all three implementations is identical and the layout only differs where it is required for the thermal implementation. This is done by using a base block that is used for all thermal test chips. This base block is repeated several times on a larger board.

The base block (Figure B.11) is 25 mm by 25 mm wide and contains one TTC in the centre of the block. In order to insulate the chip from the copper planes, there is a 10 mm x 10 mm clearance in the copper plane on all layers, except for the area underneath the chip. This copper fill is repeated on all layers (not for TTC2, where there is no copper plane above the chip). All connections are routed to the outer edges of the base block. The 4 connections for heating the chip need to be at least 200 µm wide, but the other connections can have the minimal track width of 75 µm. Pin 9 and 10 of the TTC are routed to two manual test pads of 1 mm x 1 mm. The other connections are routed to one of the 12 soldering pads (2 mm x 1 mm). The remaining chip pads, if any, are connected to the copper plane above the chip.

A special requirement of the base block is that it can be machined along three edges of the base block to thermally isolate the module from the rest of

the board (green line in Figure B.11). This base block is repeated 9 times on a 10 cm by 10 cm board in a 3 x 3 matrix. This results in 9 embedded thermal test chips per board, three times each implementation. The board will get a Ni/Au finish on the Cu. There is also no need for a solder mask.

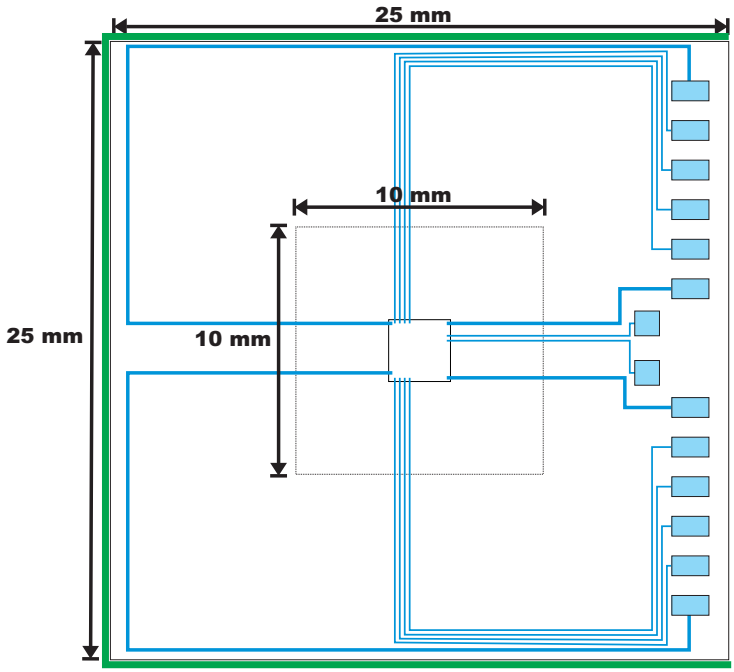


Figure B.11: Base layout block for TV2. The outline of the chip is indicated in the centre. Surrounding the chip, there is a 10 mm x 10 mm opening in the copper plane. On the right side, the soldering and contact pads are visible

TV3

When a reliable process flow has been established, more advanced technical challenges can be tackled to determine the limits of the technology. Chip embedding concepts as ultra fine pitch chips and multiple chip stacking are evaluated with the advanced technology test vehicle.

TV3 Build-up

As mentioned before, there are up to four layers of embedded chips in TV3. To obtain a very dense multi-chip package, the test vehicle uses the same thin core as for TV2. Chips are embedded in the build-up layers D1, D2, D4 and D5

Table B.5: Overview of the build-up of TV3

Layer	Type	Material	Thickness (µm)
S1	Conductor	Cu	15
D1	Dielectric	RCC	50 - 90
S2	Conductor	Cu	15
D2	Dielectric	RCC	50 - 90
S3	Conductor	Cu	17
D3	Dielectric	FR4	150
S4	Conductor	Cu	17
D4	Dielectric	RCC	50 - 90
S5	Conductor	Cu	15
D5	Dielectric	RCC	50 - 90
S6	Conductor	Cu	15

(Table B.5). Targeted chip thickness is 30 µm to 50 µm. First experiments used the 50 µm thickness, but it is possible to use thinner chips without the need for a design change. To ensure sufficient RCC height above the chip, especially with the low amount of silicon per layer, a RCC of 90 µm is again used. For the 30 µm chips this can be reduced to 50 µm. More information about the required height above the chip can be found in section refsec:process.

TV3 layout rules

The most important design rules for TV3 are shown in Table B.6. Main challenges here are the fine pitch of the chips, the landless microvia-to-chip and the fine lines and spacing on the build-up layers. The layout rules for the core layers are kept within advanced printed circuit board specifications.

TV3 components

Two different test chips are used on TV3: the IZM21.1 from TV1 and the finer pitch version IZM29. The pad size for the IZM21.1 is 100 µm, while the IZM29 pads are only 50 µm in diameter. Copper bumps (see section refsec:process) are again used to enlarge these pads, but of course the 100 µm pitch restricts the maximum diameter. The IZM21.1 can also be used as the flip-chip component.

TV3 includes several advanced technologies, which can each be tested separately. The die bonding of very large chips was moved to separate die bonding tests, since the rest of the processing is not different from the smaller chips. The use of ultra thin chips of 30 µm and beyond can also be tested on TV3, but was moved to a later stage to give priority to the fine pitch and chip stacking.

Table B.6: Layout rules for TV3

Core	(µm)
Min. Via Hole Diameter	150
Min. Via Land Diameter	400
Min. Outer Layer Track Width	75
Min. Outer Layer Spacing	75
Min. Distance Thermal Hole - Embedded Die	150
Dies	
Min. Pitch	100
Die Bond Adhesive Layer Thickness	15
Build Up Layer	
Microvia-to-core Diameter	100
Microvia-to-core Land Diameter on core	200
Microvia-to-core Land Diameter on top	200
Microvia-to-chip Diameter	30
Microvia-to-chip Land Diameter	30
Track Width	50
Clearance Track to Track	50
Clearance Track to Pad	50

Table B.7: Different daisy chain test chips used for TV3

Type	Size	I/O pitch	I/O's	FPM	dies
IZM21.1	10 x 10 mm^2	200 µm	184	16	28
IZM29	5 x 5 mm^2	100 µm	176	8	36

The multi-level stacking of embedded dies leads to a multitude of different combinations. Not only is there a need to investigate the combination of small and bigger chips, but also the effect of embedding chips on both sides of the core and the influence of an asymmetrical build-up. Eight combinations are shown in Figure B.12 for the upper two build-up layers, mixing these combinations on two sides of the core gives 16 different implementations on TV3.

One of the challenges of multi-level stacking of embedded dies is that the dies on the outer layers are placed on structured copper. In previous test vehicles, the dies were always placed on a copper plane. To be able to use the space above the dies for routing, as shown in Figure B.12, it must be possible to die bond the chips on an uneven surface, using the die bonding adhesive to fill up the spacing in between the tracks. Two types of patterns are used to test this: a bar code pattern and a daisy chain routing pattern. The lines and

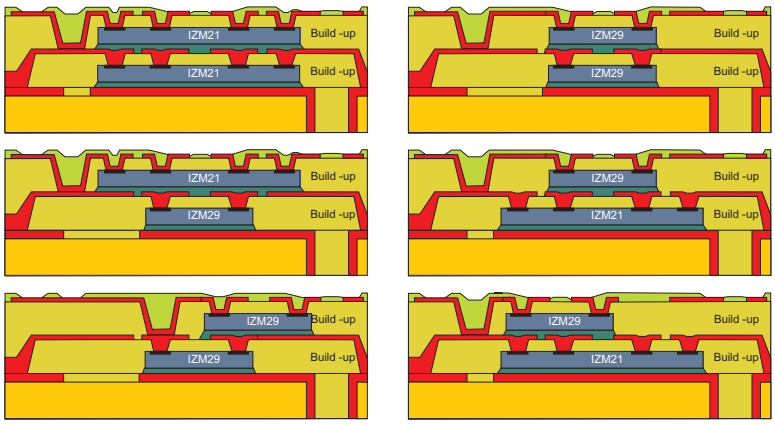


Figure B.12: Different stacking combinations implemented on TV3

spaces for the first type are 100 µm wide. This type is also implemented on the core layer, so it is possible to do the die bonding test, without completing the full build-up. The second type uses part of the daisy chain connected to the chip below as routing underneath the chip in the second build-up layer. This allows for possible defects to be electrically measured after embedding the chips.

Very fine lines and spaces are not a critical aspect in the embedding process. For this reason the minimum line width and spacing is 50 µm/50 µm. To test for the possible effect on the etching performance, some separate fine line etch test structures were added to the design.

Apart from the multi-level stacking of embedded dies, the use of small pitch test chips creates another technological challenge. The 100 µm pitch gives tight restrictions on die bonding and laser drilling accuracy. To limit the influence of board deformations, each module uses local fiducials for die bonding and laser alignment. The reduction of the via drill size to 30 µm is also necessary to accommodate to the small pitch.

Appendix C

Multilayer microstrip model - Matlab code

The actual implementation in Matlab of the final model for the multilayer microstrip, as presented in section 3.2.2, is explained here.

```
function [eps_eff,Zo,alpha,R,L,G,C] ...
= calcul_param_Si2(eps1,eps2,s2,eps3,w,h1,h2,h3,t,freq)
```

The algorithm calculates the effective dielectric constant, the characteristic impedance, the total loss and the per-unit-length parameters based on the input of the material and geometrical parameters, which are defined according to Figure C.1. The material parameters can be frequency dependent.

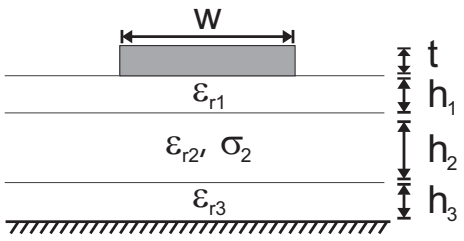


Figure C.1: Geometry for a track running on top of an embedded component. Layer 1 is the RCC, layer 2 is the silicon and layer 3 is the die bond adhesive

The code begins with initialising all the matrix variables and verifies whether or not the given material parameters are frequency dependent. After that, the Fourier transform of the trial function is calculated (`X` being the Fourier variable).

```
Fb = @(X) 8/5*sin(X*w/2)./(X*w/2) + 12./(5*(X*w/2).^2) ...
.*(cos(X*w/2) - 2*sin(X*w/2)./(X*w/2) + (sin(X*w/4)).^2./(X*w/4).^2);
```

The next step is the calculation of the capacitance when all the layers are replaced by air.

```
% Set all material parameters to "air".
e1 = 1;
e2 = 1;
e3 = 1;

% Calculate green's function
Ys = @(X) e1*((e2*((e3 + e2*tanh(X*h3).*tanh(X*h2)) ...
./(e3*tanh(X*h2) + e2*tanh(X*h3))) + e1*tanh(X*h1)) ...
./(e1 + e2*((e3 + e2*tanh(X*h3).*tanh(X*h2)) ...
./(e3*tanh(X*h2) + e2*tanh(X*h3))).*tanh(X*h1))) + 1;

% Calculate capacitance integral
INT = @(X) Fb(X).^2./(X.*Ys(X));
Co  = 1/(quadgk(INT,0,Inf)/(pi*8.854e-12));
```

Followed by a similar calculation for the complex capacitance of the multilayer structure and the extractions of the effective dielectric constant. A correction for the finite thickness t is applied before continuing.

```
for k = 1:N

e1 = eps1(k,1);
e3 = eps3(k,1);

% Set up epsilon for conductive region
e2 = eps2 - j*s2/(2*pi*freq(k)*8.854e-12);

% Calculate Green's function
Ys = @(X) e1*((e2*((e3 + e2*tanh(X*h3).*tanh(X*h2)) ...
./(e3*tanh(X*h2) + e2*tanh(X*h3))) + e1*tanh(X*h1)) ...
./(e1 + e2*((e3 + e2*tanh(X*h3).*tanh(X*h2)) ...
./(e3*tanh(X*h2) + e2*tanh(X*h3))).*tanh(X*h1))) + 1;

% Calculate capacitance integral
INT = @(X) Fb(X).^2./(X.*Ys(X));
C  = 1/(quadgk(INT,0,Inf)/(pi*8.854e-12));

% Calculate eps_eff
eps_eff(k,2) = C/Co;

% Compensate for track thickness
eps_eff(k,2) = eps_eff(k,2) ...
- (fromeff(real(eps_eff(k,2)),w,h,t) - 1)/4.6*(t/w/sqrt(w/h));

end
```

With the complex effective dielectric constant known, the characteristic impedance can be calculated next.

```
if w/h ≤ 1/(2*pi)
        We_h = w/h + 1.25/pi*t/h*(1 + log(4*pi*w/t));
    else
        We_h = w/h + 1.25/pi*t/h*(1 + log(2*h/t));
end

if w/h ≤ 1
    for k=1:N
        Zo(k,2) = 60/sqrt(real(eps_eff(k,2)))*log(8/We_h + 0.25*We_h);
    end
else
    for k=1:N
        Zo(k,2) = 120*pi/sqrt(real(eps_eff(k,2))) ...
        *(We_h + 1.393 + 0.667*log(We_h + 1.444))^-1;
    end
end
```

The dielectric loss is derived from the imaginary part of the effective dielectric constant, while the conductive loss is based on the incremental inductance rule from Wheeler. An additional roughness factor is included to more accurately model the loss at high frequencies.

```
for k=1:N
    d_Cu = 1/sqrt(pi*freq(k)*pi*4e-7*s_Cu);
    % roughness factor
    kr(k,1) = 1 + 2/pi*atan(1.4*pi*freq(k)*4e-7*pi*5.98e7*h_RMS^2);
    % Incremental inductance rule applied to impedance [D. Pozar p97]
    alpha_c(k,2) = kr(k,1)*real(pi*freq(k)/3e8 ...
    *sqrt(real(eps_eff(k,2))) ...
    *(microstrip(0,1,w - d_Cu,h + d_Cu/2,t - d_Cu) ...
    - microstrip(0,1,w,h,t))/(microstrip(0,1,w,h,t)));
    alpha_d(k,2) = pi*freq(k)/3e8*-imag(eps_eff(k,2)) ...
    /sqrt(real(eps_eff(k,2)));
end

alpha(:,2) = alpha_c(:,2) + alpha_d(:,2);
```

Before calculating the final RLGC parameters, the complex inductance for the multilayer substrate needs to be derived. This is done here by defining a series per-unit-length impedance which uses the effective width, compensated for the track thickness, and the effective height for the conductive multilayer substrate, as input. To avoid possible *divide-by-zero* issues with non-conductive layers, an extra safety switch to check if $\sigma_2 = 0$ is added.

```
% Series p.u.l. impedance of a microstrip
Zser = @(x,y) 1e-7*log(1 + 32*(y./x).^2 ...
```

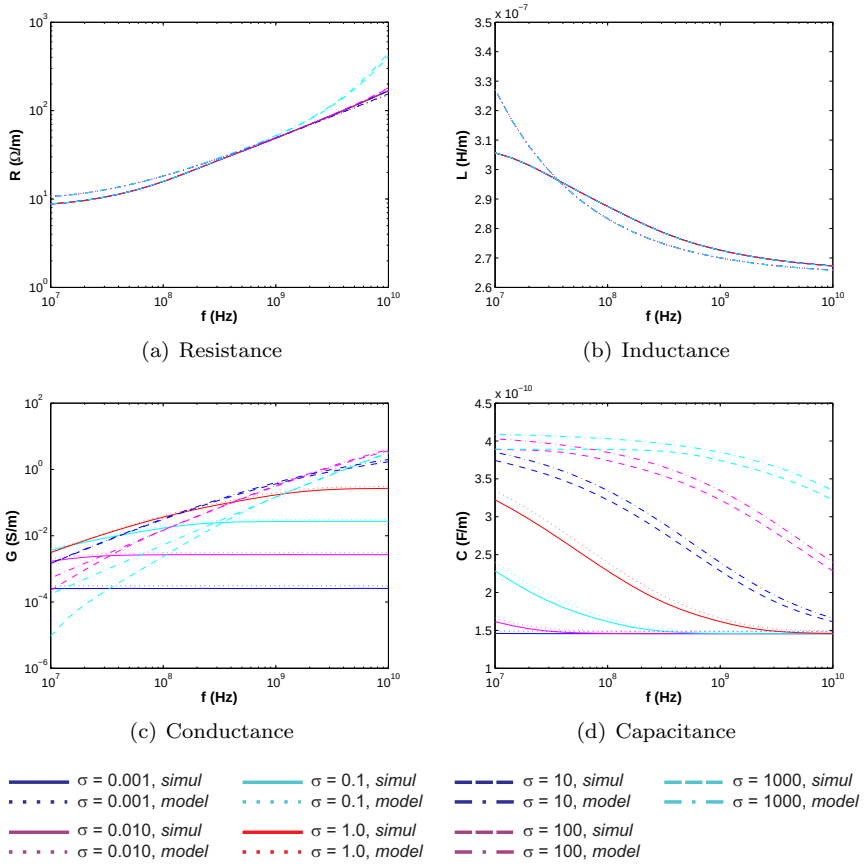
```
*(1 + sqrt(1 + (pi/8*x./y).^2)));

% Compensate for track thickness
w_eff = w + t/pi*log(4*exp(1)/sqrt((t/h)^2 + (1/(pi*(w/t + 1.10)))^2));

for k = 1:N
d_Si = 1/sqrt(pi*R(k,1)*pi*4e-7*s2);
d_Cu = 1/sqrt(pi*R(k,1)*pi*4e-7*s_Cu);
% Safety switch for s2 = 0
if s2 ~= 0
    h_eff_s = h1 + (h3 + d_Si/(1 + j)*tanh(h2/d_Si*(1 + j))) ...
    /(1 + h3/d_Si*(1 + j)*tanh(h2/d_Si*(1 + j)));
else
    h_eff_s = h;
end
% Compensate for track thickness with effective height
w_eff_s = w + t/pi*log(4*exp(1) ...
/sqrt((t/h_eff_s)^2 + (1/(pi*(w/t + 1.10)))^2));

% Resistive loss in conductive region
R_Si(k,1) = -2*pi*R(k,1)*imag(Zser(w_eff_s,h_eff_s));
alpha_s(k,2) = R_Si(k,1)/(2*real(Zo(k,2)));

% roughness factor for R_Cu
kr(k,1) = 1 + 2/pi*atan(1.4*pi*freq(k)*4e-7*pi*5.98e7*h_RMS^2);
R_Cu(k,1) = sqrt(1/(s_Cu*w*t)^2 +  (2*pi*R(k,1)/3e8*kr(k,1) ...
*(microstrip(0,1,w - d_Cu,h + d_Cu/2,t - d_Cu) ...
- microstrip(0,1,w,h,t)))^2);
% sqrt(R_dc^2 + R_ac^2) according to H. Johnson (p. 72)
end
```

Finally the per-unit-length conductance, capacitance, resistance and inductance are calculated.

```
G(k,2) = 2*alpha_d(k,2)/real(Zo(k,2));
C(k,2) = sqrt(real(eps_eff(k,2)))/real(Zo(k,2))/3e8;
R(k,2) = R_Si(k,1) + real(R_Cu(k,1));
L(k,2) = real(Zser(w_eff_s,h_eff_s)) ...
+ (Zser(w_eff - d_Cu,h + d_Cu/2) - Zser(w_eff,h));
% Lext with effective height + internal inductance with skin effect
```

Appendix D

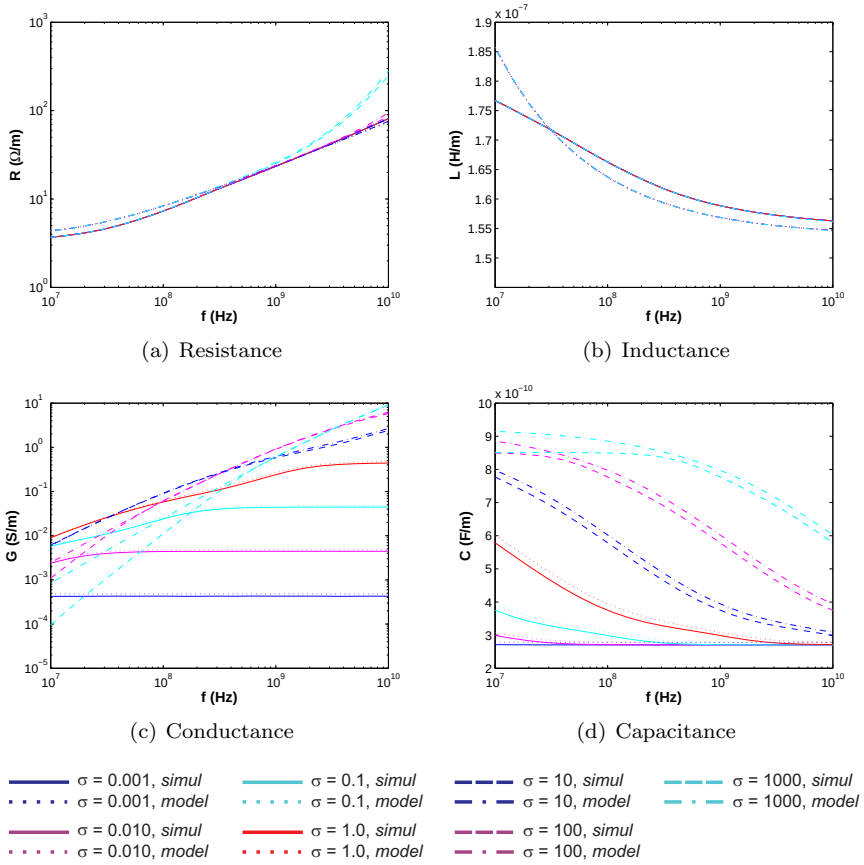
Comparison between simulation and model



(a) Resistance (b) Inductance

(c) Conductance (d) Capacitance

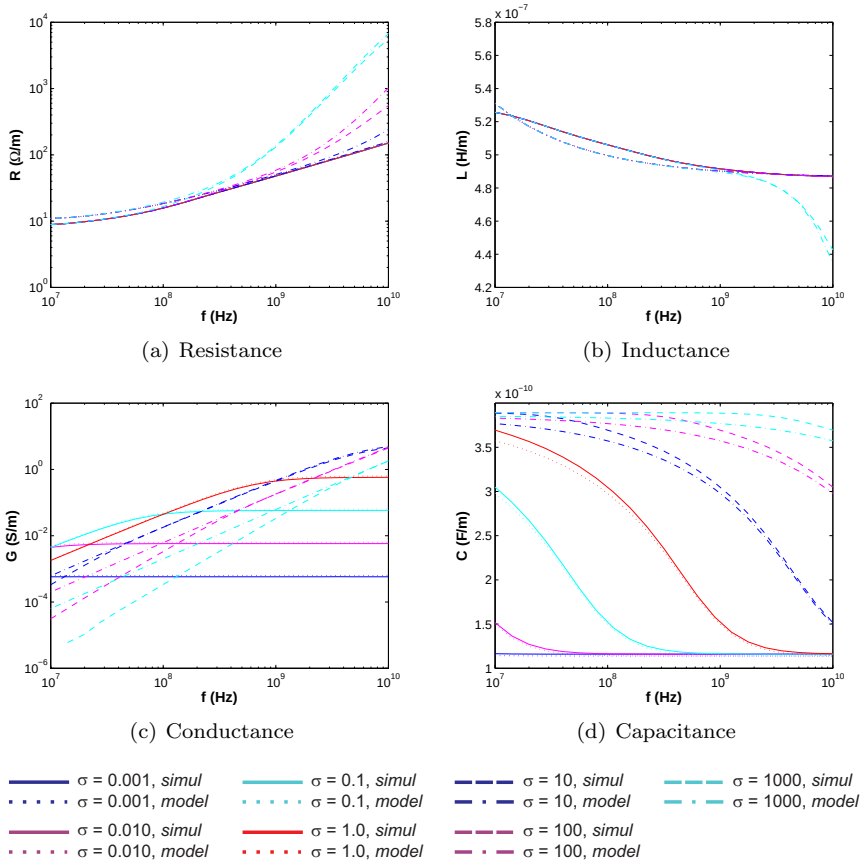
Figure D.1: Comparison between simulation results and the final model. All conductivity values in S/m ($w = 100\,\mu\text{m}$, $h_1 = 10\,\mu\text{m}$, $h_2 = 20\,\mu\text{m}$, $h_3 = 20\,\mu\text{m}$ and $t = 20\,\mu\text{m}$)



(a) Resistance (b) Inductance

(c) Conductance (d) Capacitance

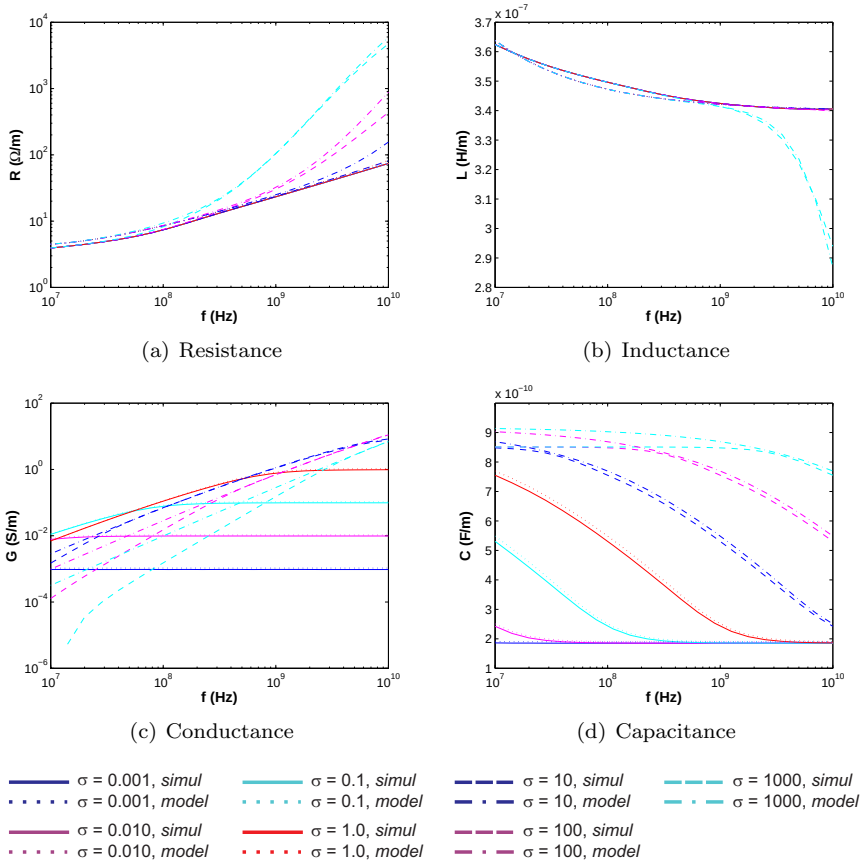
Figure D.2: Comparison between simulation results and the final model. All conductivity values in S/m ($w = 250\,\mu\text{m}$, $h_1 = 10\,\mu\text{m}$, $h_2 = 20\,\mu\text{m}$, $h_3 = 20\,\mu\text{m}$ and $t = 20\,\mu\text{m}$)



(a) Resistance (b) Inductance

(c) Conductance (d) Capacitance

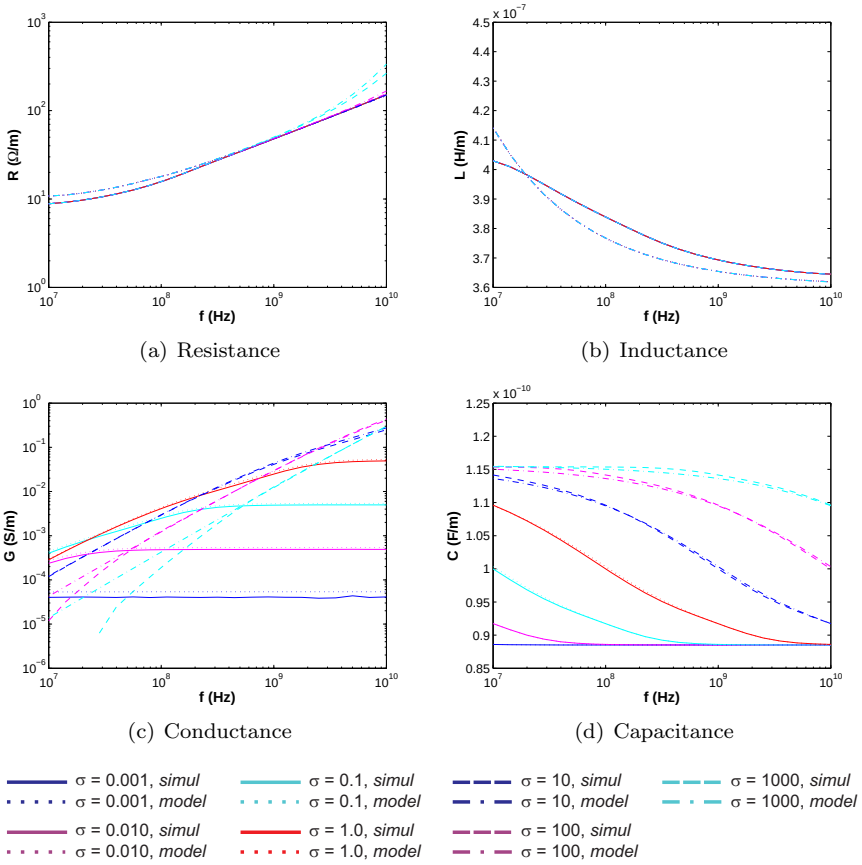
Figure D.3: Comparison between simulation results and the final model. All conductivity values in S/m ($w = 100\,\mu\text{m}$, $h_1 = 10\,\mu\text{m}$, $h_2 = 150\,\mu\text{m}$, $h_3 = 20\,\mu\text{m}$ and $t = 20\,\mu\text{m}$)



(a) Resistance (b) Inductance

(c) Conductance (d) Capacitance

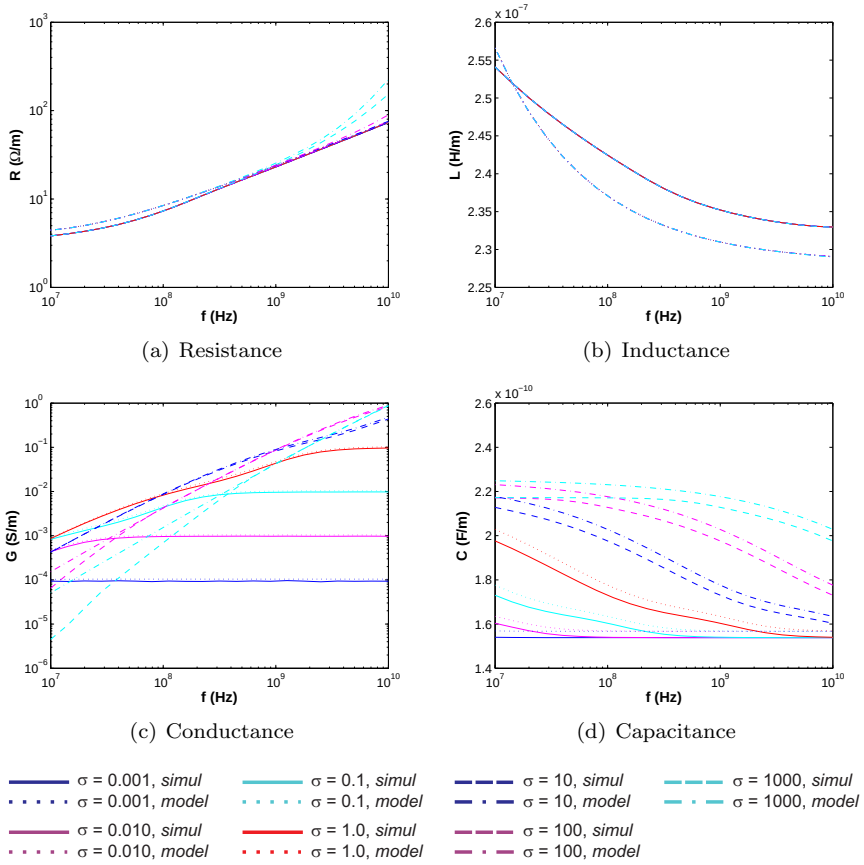
Figure D.4: Comparison between simulation results and the final model. All conductivity values in S/m ($w = 250\,\mu\text{m}$, $h_1 = 10\,\mu\text{m}$, $h_2 = 150\,\mu\text{m}$, $h_3 = 20\,\mu\text{m}$ and $t = 20\,\mu\text{m}$)



(a) Resistance (b) Inductance

(c) Conductance (d) Capacitance

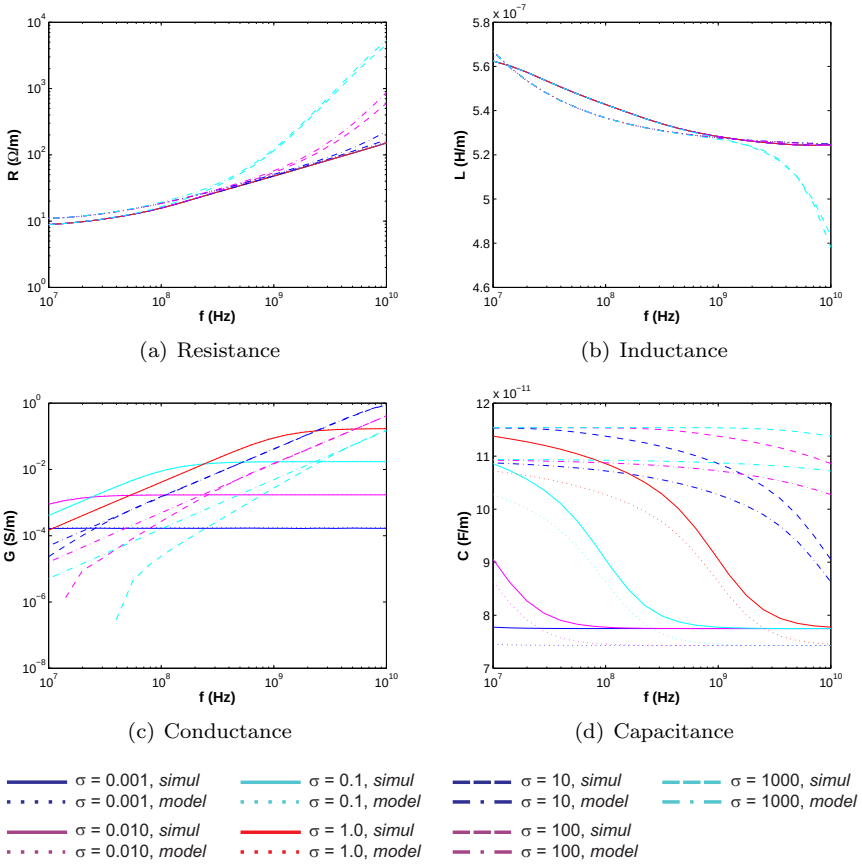
Figure D.5: Comparison between simulation results and the final model. All conductivity values in S/m ($w = 100\,\mu\text{m}$, $h_1 = 50\,\mu\text{m}$, $h_2 = 20\,\mu\text{m}$, $h_3 = 20\,\mu\text{m}$ and $t = 20\,\mu\text{m}$)



(a) Resistance (b) Inductance

(c) Conductance (d) Capacitance

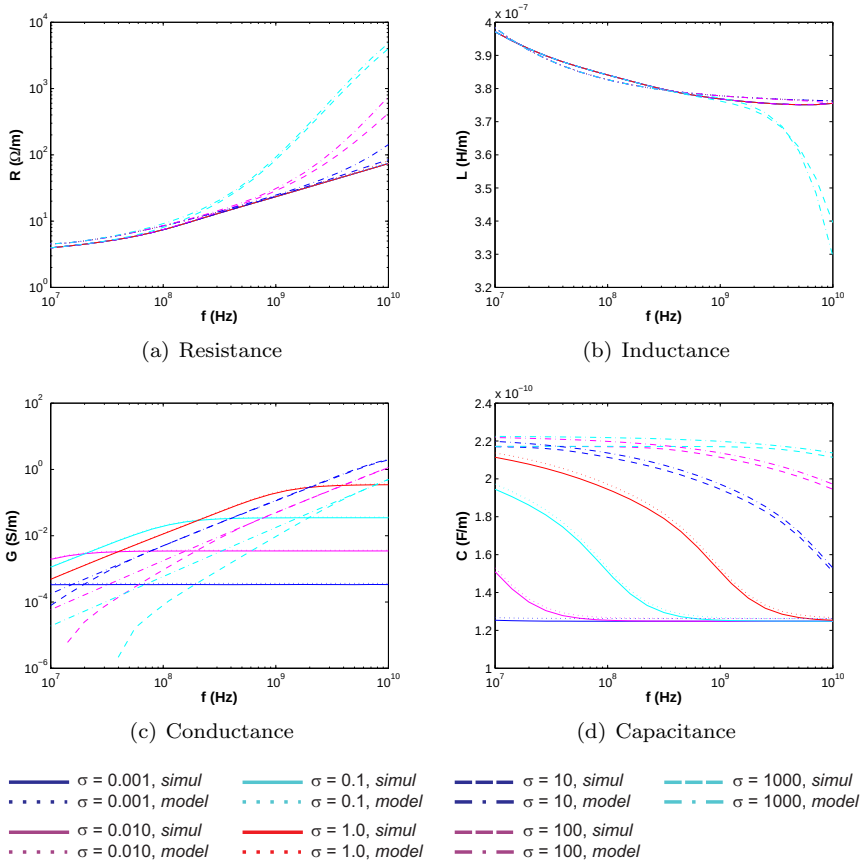
Figure D.6: Comparison between simulation results and the final model. All conductivity values in S/m ($w = 250\,\mu\text{m}$, $h_1 = 50\,\mu\text{m}$, $h_2 = 20\,\mu\text{m}$, $h_3 = 20\,\mu\text{m}$ and $t = 20\,\mu\text{m}$)



(a) Resistance (b) Inductance

(c) Conductance (d) Capacitance

Figure D.7: Comparison between simulation results and the final model. All conductivity values in S/m ($w = 100\,\mu\text{m}$, $h_1 = 50\,\mu\text{m}$, $h_2 = 150\,\mu\text{m}$, $h_3 = 20\,\mu\text{m}$ and $t = 20\,\mu\text{m}$)



(a) Resistance (b) Inductance

(c) Conductance (d) Capacitance

Figure D.8: Comparison between simulation results and the final model. All conductivity values in S/m ($w = 250\,\mu\text{m}$, $h_1 = 50\,\mu\text{m}$, $h_2 = 150\,\mu\text{m}$, $h_3 = 20\,\mu\text{m}$ and $t = 20\,\mu\text{m}$)

Appendix E

Multiline TRL Matlab code

While the mathematical background of the multiline TRL (ML-TRL) algorithm has been explained in section 4.2, this appendix shows the actual implementation in Matlab. This "translation" is not always straight-forward and incorrect assumptions may lead to spikes in the corrected S-parameters or discontinuities in the extracted propagation constant. A great help was the conference paper on implementing the ML-TRL algorithm by D.C. DeGroot [99].

```
function [gamma,X,Y_bar] = multiTRLX(eps_eff_est,tan_D_est)
```

The only input, apart from the measurement data, that is required is an estimate of the effective dielectric constant ϵ_{eff} and the loss tangent $\tan\delta$. The accuracy of the extracted propagation constant γ is not really sensitive to this input, however an incorrect value will result in jumps in the imaginary part of γ. A good initial value can be obtained from the phase shift of the longest line ($\angle S_{21} = \frac{2\pi f}{c}\sqrt{\epsilon_{eff}}l$).

```
O = input('Please enter the number of line standards: ');
P = sum(1:O-1);

current_dir = pwd;

for k = 1:O
    cd('C:\Documents and Settings\mcauwe\My Documents\meting');
    [file,path] = uigetfile('*.*','Loading standard measurement file');
    cd(current_dir);
    LINE(:,:,k) = import_s2p(strcat(path,file),6);
    disp(strcat('The following standard was loaded:',file));
    lengths(k) = input('Please provide the length the standard (m): ');
end

```

```
cd('C:\Documents and Settings\mcauwe\My Documents\meting');
[file_R1,path_R1]=uigetfile('*.*','Select the 1st Reflect standard');
[file_R2,path_R2]=uigetfile('*.*','Select the 2nd Reflect standard');
cd(current_dir);
REFLECT1 = import_s2p(strcat(path_R1,file_R1),6);
disp(strcat('The following standard was loaded:',file_R1));
REFLECT2 = import_s2p(strcat(path_R2,file_R2),6);
disp(strcat('The following standard was loaded:',file_R2));

N = length(LINE);
```

The first thing that needs to be done is to import all the measurement data form the different calibration standards. The code can accept any number of line standards (including the THRU standard) and up to two reflection standards. The length of the REFLECT standards are assumed to be half that of the THRU standard. When all the data is imported, the variables used in the rest of the code are preloaded into memory to improve the speed of the calculations.

```
gamma_est(1:N,2) = j*2*pi*gamma_est(1:N,1)/3e8*sqrt(eps_eff_est) ...
                   *(1 - j*tan_D_est);

n = 1;
for k = 1:O-1
    for l = 1:O-k
        D_lengths(n) = lengths(l+k) - lengths(k);
        n = n + 1;
    end
end
```

An estimation for the propagation constant γ is calculated based on the input values for the dielectric constant and the loss tangent. It is used to calculate the effective phase differences and to correct jumps in the extracted propagation constant. The two nested *for* loops are used to set up the length differences in the correct order.

```
for i=1:N
    for k = 1:O-1
        for l = 1:O-k
            phi_pairs(l) = real(asin(abs( ...
            exp(-gamma_est(i,2)*(lengths(l+k)-lengths(k))) ...
            - exp(gamma_est(i,2)*(lengths(l+k) - lengths(k))))/2));
        end
        phi_T(i,k) = min(phi_pairs);
        clear phi_pairs
    end
end

for i=1:N
    [phi_eff(i,1),common_line(i,1)] = max(phi_T(i,:));
end
```

In the paper, the algorithm continues with the determination of the optimal *common line* for each frequency point. Since any of the line standards can be used as the common line for each line pair, the choice of this common line is used to maximize the accuracy at each frequency point. The highest accuracy is obtained when the phase difference between two lines is close to 90 degrees. For each frequency point, the ML-TRL algorithm calculates the phase difference for all the line pairs using the a given common line. From all these phase differences, the lowest value is selected, representing the line pair that would give the largest calibration error at this frequency. This is repeated for all of the other line standards used as common line. Among all of these minimum phase differences, the largest value is selected and the corresponding line standard represents the optimal common line for that frequency point.

```
for k=1:O
    TLINE(:,:,k) = stot(LINE(:,:,k));
end

n = 1;
for k = 1:O-1
    for l = 1:O-k
        line_pairs(:,:,n) = mulT(TLINE(:,:,l+k),TLINE(:,:,k),0,1);
        n = n + 1;
    end
end

for k=1:P
    for i=1:N
        M(1,1) = line_pairs(i,2,k);
        M(1,2) = line_pairs(i,4,k);
        M(2,1) = line_pairs(i,3,k);
        M(2,2) = line_pairs(i,5,k);
        d = eig(M);
        eigen_values(i,2,k) = d(1,1);
        eigen_values(i,3,k) = d(2,1);
    end
end
```

The measured S-parameters are converted to cascade parameters, which are used to calculate the line pairs. Only lines that are longer than the common line are used to create the line pairs, since these combinations are already included in other pairs (line pair (L1,L2) is equivalent to line pair (L2,L1)). Each line pair results in two eigenvalues, according to the eigenvalue equation 4.4. The paper from DeGroot uses an analytical expression to calculate the eigenvalues, however the numerical algorithm included with Matlab (*eig*) has less issues with complex numbers and does not require the elaborate selection mechanism explained in the paper.

```
for l=1:P
        for n=1:P
            if l == n
                Vs(l,n) = 1 - 1/(P+1);
            else
                Vs(l,n) = -1/(P+1);
            end
        end
end

for k=1:P
    for i=1:N
        Ea = (eigen_values(i,2,k) + 1/eigen_values(i,3,k))/2;
        gamma_DL(i,2,k) = -log(Ea) + j*2*pi*round(( ...
        imag(gamma_est(i,2)*D_lengths(k)) - imag(-log(Ea)))/(2*pi));
    end
end

L = D_lengths';

for i=1:N
    for k=1:P
        G(k,1) = gamma_DL(i,2,k);
    end
    gamma(i,2) = L'*Vs*G/(L'*Vs*L);
end
```

The approach to compute the best estimate of gamma from all the observations from the different line pairs, is again slightly different from the paper. De Groot et al. use a Gauss-Markov weighting matrix to obtain a best, linear, unbiased estimator. To ensure stochastically independent observations of $\gamma\Delta l$, only one set of line pairs is selected using the optimal common line at each frequency point. This method gives very accurate results, but requires all the line standards to have identical propagating behaviour. If, for example, due to manufacturing tolerances or variation in material parameters, the propagation constant for one line is slightly different from another line, this will introduce small jumps in the final result for the extracted propagation constant. By combining all the observations from all the line pairs (except the equivalent ones), the algorithm explained here obtains one average value for the extracted propagation constant without jumps. While it might not classify as a "best estimation", the resulting propagation constant is exactly the same for ideal line standards obtained from simulation.

To determine the material parameters using the ML-TRL algorithm, the extracted propagation constant is all that is required. For de-embedding purposes, or to implement the full calibration, the error box parameters X and $\bar{Y}$

can be calculated.

$$X = R_1 \begin{bmatrix} A_1 & B_1 \\ C_1 & 1 \end{bmatrix} \tag{E.1}$$

$$\bar{Y} = R_2 \begin{bmatrix} A_2 & C_2 \\ B_1 & 1 \end{bmatrix} \tag{E.2}$$

The calculations are set up in such a way to make optimal use of the symmetry between the two ports and use analytical expressions where possible. Thanks to the accuracy and stability of the numerical implementations in Matlab, the code explained here is often more simplified and straight-forward. In the paper, a new matrix τ is introduced to calculate the two off-axis terms B_i and C_i to avoid the common $1/S_{21}^j S_{12}^i$ factor. The eigenvalues for this new matrix are used in the expression for B and C/A, with are mathematically identical to the expression below using the original line pair matrix M.

$$\begin{bmatrix} M_{11}^{ij} & M_{12}^{ij} \\ M_{21}^{ij} & M_{22}^{ij} \end{bmatrix} \begin{bmatrix} 1 & B_1 \\ \frac{C_1}{A_1} & 1 \end{bmatrix} = \begin{bmatrix} 1 & B_1 \\ \frac{C_1}{A_1} & 1 \end{bmatrix} \begin{bmatrix} \lambda_1^{ij} & 0 \\ 0 & \lambda_2^{ij} \end{bmatrix} \tag{E.3}$$

Which results in the following equations.

$$B_1^a = \frac{M_{12}^{ij}}{\lambda_1^{ij} - M_{11}^{ij}} \tag{E.4}$$

$$\frac{C_1}{A_1}^a = \frac{M_{21}^{ij}}{\lambda_2^{ij} - M_{22}^{ij}} \tag{E.5}$$

$$B_1^b = \frac{\lambda_1^{ij} - M_{22}^{ij}}{M_{21}^{ij}} \tag{E.6}$$

$$\frac{C_1}{A_1}^b = \frac{\lambda_2^{ij} - M_{11}^{ij}}{M_{12}^{ij}} \tag{E.7}$$

Since it is not possible to tell which of the eigenvalues calculated by Matlab corresponds to λ_1 or λ_2, each of the expressions above can be evaluated using λ_1 instead of λ_2 or vice versa. To choose the correct one, the algorithm compares the two cases to estimates based on the extracted propagation constant. The case closest to these estimates becomes the observation of B and C/A.

```
1 for k=1:P
2   for i=1:N
3     B1_a1=line_pairs(i,4,k)/(eigen_values(i,2,k)-line_pairs(i,2,k));
4     CA1_a1=line_pairs(i,3,k)/(eigen_values(i,3,k)-line_pairs(i,5,k));
5     B1_a2=line_pairs(i,4,k)/(eigen_values(i,3,k)-line_pairs(i,2,k));
6     CA1_a2=line_pairs(i,3,k)/(eigen_values(i,2,k)-line_pairs(i,5,k));
7     B1_b1=(eigen_values(i,2,k)-line_pairs(i,5,k))/line_pairs(i,3,k);
8     CA1_b1=(eigen_values(i,3,k)-line_pairs(i,2,k))/line_pairs(i,4,k);
```

```
9       B1_b2=(eigen_values(i,3,k)-line_pairs(i,5,k))/line_pairs(i,3,k);
10      CA1_b2=(eigen_values(i,2,k)-line_pairs(i,2,k))/line_pairs(i,4,k);
11
12      B_est_a = line_pairs(i,4,k) ...
13      /(exp(gamma(i,2)*D_lengths(k)) - line_pairs(i,2,k));
14      B_est_b = (exp(gamma(i,2)*D_lengths(k)) - line_pairs(i,5,k)) ...
15      /line_pairs(i,3,k);
16      CA_est_a = line_pairs(i,3,k) ...
17      /(exp(-gamma(i,2)*D_lengths(k)) - line_pairs(i,5,k));
18      CA_est_b = (exp(-gamma(i,2)*D_lengths(k))-line_pairs(i,2,k)) ...
19      /line_pairs(i,4,k);
20
21      [min_B l] = min([abs(B1_a1 - B_est_a) abs(B1_a2 - B_est_a) ...
22      abs(B1_b1 - B_est_b) abs(B1_b2 - B_est_b)]);
23      if l == 1
24          B1(i,k) = B1_a1;
25      end
26      if l == 2
27          B1(i,k) = B1_a2;
28      end
29      if l == 3
30          B1(i,k) = B1_b1;
31      end
32      if l == 4
33          B1(i,k) = B1_b2;
34      end
35      [min_C l] = min([abs(CA1_a1-CA_est_a) abs(CA1_a2-CA_est_a) ...
36      abs(CA1_b1-CA_est_b) abs(CA1_b2-CA_est_b)]);
37      if l == 1
38          CA1(i,k) = CA1_a1;
39      end
40      if l == 2
41          CA1(i,k) = CA1_a2;
42      end
43      if l == 3
44          CA1(i,k) = CA1_b1;
45      end
46      if l == 4
47          CA1(i,k) = CA1_b2;
48      end
49    end
50  end
```

For port 2, the calculations in the paper take advantage of the symmetry by exchanging the port indices on the S-parameters used to form the matrix τ. In the same manner the eigenvalue equation for the error box X at port 1 was obtained, an equivalent equation can be obtained for $\bar{Y}$ at port 2.

$$\left(M^{ij}\right)^{-1} = \left(M^{j}\right)^{-1} M^{i} = \bar{Y}^{-1} \left(T^{j}\right)^{-1} X^{-1} X T^{i} \bar{Y} \tag{E.8}$$

Left-multiplication with $\bar{Y}$ gives

$$\bar{Y} \left(M^{ij}\right)^{-1} = \left(T^{ij}\right)^{-1} \bar{Y} \tag{E.9}$$

By taking the transpose of both sides of the equation, a new eigenvalue equation is obtained. The *rows* of $\bar{Y}$ are the eigenvectors of the inverse of M^{ij} and the eigenvalues of $\left(M^{ij}\right)^{-1}$ are the inverse of the eigenvalues of M^{ij}.

$$\begin{bmatrix} M_{11}^I & M_{21}^I \\ M_{12}^I & M_{22}^I \end{bmatrix} \begin{bmatrix} 1 & B_2 \\ \frac{C_2}{A_2} & 1 \end{bmatrix} = \begin{bmatrix} 1 & B_2 \\ \frac{C_2}{A_2} & 1 \end{bmatrix} \begin{bmatrix} \lambda_1^{-1} & 0 \\ 0 & \lambda_2^{-1} \end{bmatrix} \tag{E.10}$$

The superscripted I denotes the elements of the inverted matrix. After expansion, this results in similar expressions as for port 1.

$$B_2^a = \frac{M_{21}^I}{\lambda_2^{-1} - M_{11}^I} \tag{E.11}$$

$$\frac{C_2}{A_2}^a = \frac{M_{12}^I}{\lambda_1^{-1} - M_{22}^I} \tag{E.12}$$

$$B_2^b = \frac{\lambda_2^{-1} - M_{22}^I}{M_{12}^I} \tag{E.13}$$

$$\frac{C_2}{A_2}^b = \frac{\lambda_1^{-1} - M_{11}^I}{M_{21}^I} \tag{E.14}$$

After the calculation of the inverted matrix and the eigenvalues, the code is completely similar to port 1. For this reason, it is omitted here.

```
for k=1:P
    tau_line_pairs(:,:,k) = invT(line_pairs(:,:,k));
    tau_eigenv(:,2:3,k) = 1./(eigen_values(:,2:3,k));
end
```

As was the case for the propagation constant, all the different observations of the off-axis elements need to be combined to obtain one final estimate for B and C/A. In contrast to the propagation constant, not all the observations can be combined, since it is not possible to construct a general measurement noise covariance matrix V. For each common line, a different covariance matrix is constructed and numerically inverted. As it is clear from the code below, covariance matrix depends on the extracted propagation constant, the length of the common line and the lengths of the other lines in the pairs.

```
for i=1:N
    m = 1;
    r = 1;
    for k = 1:O-1
        for l = 1:O-k
            B_1(l,1) = B1(i,r);
            B_2(l,1) = B2(i,r);
            CA_1(l,1) = CA1(i,r);
```

```
            CA_2(l,1) = CA2(i,r);
            r = r + 1;
        end
        for l = 1:O-k
          for n = 1:O-k
            if l == n
                VB(l,n) = (abs(exp(-gamma(i,2)*D_lengths(m)))^2 ...
                + abs(exp(-gamma(i,2)*D_lengths(m)))^-2 ...
                + 2*(abs(exp(-gamma(i,2)*length(n+k))) ...
                *abs(exp(-gamma(i,2)*length(k))))^2) ...
                /(abs(exp(-gamma(i,2)*D_lengths(m)) ...
                - exp(gamma(i,2)*D_lengths(m)))^2);
                VC(l,n) = (abs(exp(-gamma(i,2)*D_lengths(m)))^2 ...
                + abs(exp(-gamma(i,2)*D_lengths(m)))^-2 ...
                + 2*(abs(exp(-gamma(i,2)*length(n+k))) ...
                *abs(exp(-gamma(i,2)*length(k))))^-2) ...
                /(abs(exp(-gamma(i,2)*D_lengths(m)) ...
                - exp(gamma(i,2)*D_lengths(m)))^2);
            else
                VB(l,n) = (exp(-gamma(i,2)*D_lengths(m)) ...
                *(exp(-gamma(i,2)*D_lengths(m+n-l)))' ...
                + abs(exp(-gamma(i,2)*length(k)))^2 ...
                *exp(-gamma(i,2)*length(l+k)) ...
                *(exp(-gamma(i,2)*length(n+k)))') ...
                /((exp(-gamma(i,2)*D_lengths(m)) ...
                - exp(gamma(i,2)*D_lengths(m))) ...
                *(exp(-gamma(i,2)*D_lengths(m+n-l)) ...
                - exp(gamma(i,2)*D_lengths(m+n-l)))');
                VC(l,n) = ((exp(-gamma(i,2)*D_lengths(m)) ...
                *(exp(-gamma(i,2)*D_lengths(m+n-l)))')^-1 ...
                + abs(exp(-gamma(i,2)*length(k)))^2 ...
                *exp(-gamma(i,2)*length(l+k)) ...
                *(exp(-gamma(i,2)*length(n+k)))')^-1 ...
                /((exp(-gamma(i,2)*D_lengths(m)) ...
                - exp(gamma(i,2)*D_lengths(m))) ...
                *(exp(-gamma(i,2)*D_lengths(m+n-l)) ...
                - exp(gamma(i,2)*D_lengths(m+n-l)))');
            end
            if l > n
                VB(l,n) = VB(l,n)';
                VC(l,n) = VC(l,n)';
            end
          end
        m = m + 1;
        end
        H = ones(O-k,1);
        B1_final(i,k) = H'*VB^-1*B_1/(H'*VB^-1*H);
        B2_final(i,k) = H'*VB^-1*B_2/(H'*VB^-1*H);
        CA1_final(i,k) = H'*VC^-1*CA_1/(H'*VC^-1*H);
        CA2_final(i,k) = H'*VC^-1*CA_2/(H'*VC^-1*H);
        clear B_1 B_2 CA_1 CA_2 H VB VC
    end
end
```

The last step in the ML-TRL algorithm is to calculate the on-axis terms, A_i and R_i, using the measurements from the REFLECT standards. If multiple reflection standards are available, an average value of A can be obtained, however only a single reflection standard is required for the algorithm.

```
for k=1:O-1
  for i=1:N
      Ap=-((B1_final(i,k)*-B2_final(i,k)-B1_final(i,k)*LINE(i,5,1) ...
      + B2_final(i,k)*LINE(i,2,1) + LINE(i,2,1)*LINE(i,5,1) ...
      - LINE(i,3,1)*LINE(i,4,1))/(1 - CA1_final(i,k)*LINE(i,2,1) ...
      + CA2_final(i,k)*LINE(i,5,1)+CA1_final(i,k)*-CA2_final(i,k) ...
      *(LINE(i,2,1)*LINE(i,5,1) - LINE(i,3,1)*LINE(i,4,1))));

      Ar = (REFLECT1(i,2) - B1_final(i,k)) ...
      /(1 - REFLECT1(i,2)*CA1_final(i,k)) ...
      *(1 - REFLECT1(i,5)*-CA2_final(i,k)) ...
      /(REFLECT1(i,5) + B2_final(i,k));

      % Take the value of REFLECT at f_start as estimate for
      % the reflection coefficient of the reflect
      Rr_est = REFLECT1(1,2);


      R_trial = (REFLECT1(i,2) - B1_final(i,k)) ...
      /(sqrt(Ap*Ar)*(1 - REFLECT1(i,2)*CA1_final(i,k)));

      mag_test = abs(Rr_est/abs(Rr_est) - R_trial/abs(R_trial));

      if mag_test > sqrt(2)
          A11 = -sqrt(Ap*Ar);
      else
          A11 = sqrt(Ap*Ar);
      end

      A21 = A11/Ar;

      Ar = (REFLECT2(i,2) - B1_final(i,k)) ...
      /(1 - REFLECT2(i,2)*CA1_final(i,k)) ...
      *(1 + REFLECT2(i,5)*CA2_final(i,k)) ...
      /(REFLECT2(i,5) + B2_final(i,k));

      % Take the value of REFLECT at f_start as estimate for
      % the reflection coefficient of the reflect
      Rr_est = REFLECT2(1,2);

      R_trial = (REFLECT2(i,2) - B1_final(i,k)) ...
      /(sqrt(Ap*Ar)*(1 - REFLECT2(i,2)*CA1_final(i,k)));

      mag_test = abs(Rr_est/abs(Rr_est) - R_trial/abs(R_trial));

      if mag_test > sqrt(2)
          A12 = -sqrt(Ap*Ar);
```

```
48        else
49            A12 = sqrt(Ap*Ar);
50        end
51
52        A22 = A12/Ar;
53
54        A1(i,k) = (A11 + A12)/2;
55        A2(i,k) = (A21 + A22)/2;
56
57        R1(i,k) = sqrt((TLINE(i,2,1)*TLINE(i,5,1) ...
58        - TLINE(i,3,1)*TLINE(i,4,1)) ...
59        /(A1(i,k)*(1 - B1_final(i,k)*CA1_final(i,k))));
60
61        R2(i,k) = sqrt((TLINE(i,2,1)*TLINE(i,5,1) ...
62        - TLINE(i,3,1)*TLINE(i,4,1)) ...
63        /(A2(i,k)*(1 - B2_final(i,k)*CA2_final(i,k))));
64    end
65 end
```

The coefficients A_1 and A_2 are determined from the product $A_p = A_1 A_2$ and the ratio $A_r = A_1/A_2$. The product A_p is determined from the measurement of the THRU standard and the ratio A_r is calculated from the REFLECT standard. The THRU standard is regarded as the connection of the two ports at the measurement reference plane and using this assumption, the coefficients R_i are obtained. Now all the coefficients are known and the error box matrices can be constructed.

```
1  for k=1:O-1
2      for i=1:N
3          X(i,2,k) = R1(i,k)*A1(i,k);
4          X(i,3,k) = X(i,2,k)*CA1_final(i,k);
5          X(i,4,k) = R1(i,k)*B1_final(i,k);
6          X(i,5,k) = R1(i,k);
7
8          Y_bar(i,2,k) = R2(i,k)*A2(i,k);
9          Y_bar(i,3,k) = R2(i,k)*B2_final(i,k);
10         Y_bar(i,4,k) = Y_bar(i,2,k)*CA2_final(i,k);
11         Y_bar(i,5,k) = R2(i,k);
12     end
13 end
```

It is important to note that the reference plane for the calibration is located at the centre of the THRU standard and the reference impedance for the cascade parameters of the error boxes is the characteristic impedance of the line standards. In order to use the error boxes for de-embedding purposes, the reference impedance of the error boxes needs to be transformed to the reference impedance of the measured structure. The required formulae can be found in the conference paper [99].

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